1/4-Inch 1.3-Megapixel SOC CMOS Digital Image Sensor

MT9M112 For the latest data sheet, please visit www.sunnywale.com

Features

- Micron® DigitalClarity™ CMOS imaging technology
- System-On-a-Chip (SOC)—Completely integrated camera system
- Ultra-low power, low cost, progressive scan CMOS image sensor
- On-die phase lock loop (PLL)
- Superior low-light performance
- On-die image flow processor (IFP) performs sophisticated processing: Color recovery and correction, sharpening, gamma correction, lens shading correction, and on-the-fly defect correction
- Programmable I/O slew rate
- 2 x 2 pixel binning
- Mechanical shutter support
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Fully automatic Xenon- and LED-type flash support
- Automatic Features:
  Auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, and auto defect identification and correction
- Multiple parameter contexts, easy/fast mode switching
- Camera control sequencer automates snapshots, snapshots with flash, and video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats
- VDD power disable switch for reduced standby current
- Four general purpose input bond pads

Applications

- Cellular phones
- PDAs
- Toys
- Other battery-powered products

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/4-inch (5:4)
Active imager size		3.58mm(H) x 2.87mm(V) 4.59mm diagonal
Active pixels		1280H x 1024V
Pixel size		2.8µm x 2.8µm
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		27 MPS/54 MHz
Frame rate		15 fps at full resolution, 30 fps in preview mode (640 x 512)
ADC resolution		10-bit, on-chip
Responsivity		1.0V/lux-sec (550nm)
Dynamic range		68dB
SNR_{MAX}		44dB
Supply voltage	I/O digital	1.7V–3.1V
	Core digital	1.7V–1.9V (1.8V nominal)
	Analog	2.5V–3.1V (2.8V nominal)
Power consumption		170mW at 15 fps, full resolution 100mW at 30fps, preview mode
Operating junction temperature		-30°C to +70°C
Packaging		Die

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9M112D00STC	Die

Table of Contents

List of Tables

List of Figures

General Description

The Micron® Imaging MT9M112 is an SXGA-format, single-chip camera CMOS active-pixel digital image sensor. This device combines the 2.8µm image sensor core with fourth-generation digital image flow processor technology from Micron Imaging. It captures high-quality color images at SXGA resolution.

The SXGA CMOS image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity), while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete solution designed specifically to meet the low-power, low-cost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9M112 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations, special camera effects such as sepia tone and solarization, and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both Xenon and LED-type flash light sources in several snapshot modes. The device also has an on-board PLL, and supports pixel binning as an enhanced form of image size reduction.

The MT9M112 can be programmed to output progressive-scan images up to 30 fps. The image data can be output in any one of six 8-bit formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated signals, along with a pixel clock that is synchronous with valid data.

Functional Overview

The MT9M112 is a fully-automatic, single-chip camera that requires only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8-bit DOUT port as shown in Figure 1 on page 9. The output pixel clock is used to latch data, while FRAME_VALID and LINE_VALID signals indicate the active video. The MT9M112 internal registers are configured using a two-wire serial interface.

The device can be put in a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry in standby mode also can be achieved through the two-wire serial interface register writes.

The MT9M112 accepts input clocks up to 54 MHz, delivering up to 30 fps for VGA resolution images.

Internal Architecture

Internally, the MT9M112 consists of a sensor core and an image flow processor (IFP). The IFP is divided in two sections: the colorpipe (CP) and the camera controller (CC). The sensor core captures raw Bayer-encoded images that are then input in the IFP. The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance and to support snapshot modes. The sensor core, CP, and CC registers are grouped in three separate address spaces as shown in Figure 2 on page 9.

When accessing internal registers through the two-wire serial interface, select the desired address space by programming the R0xF0 (R240) register.

The MT9M112 accelerates mode-switching with hardware-assisted context switching and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9M112 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

- Standard FRAME_VALID/LINE_VALID video interface with gated pixel clocks
- ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocks

Register Notation

The following register address notations are used in this document:

- R<decimal address>:<address page>
  Example: R9:0—Shutter width register (register 9) in the sensor page (page 0). Used to uniquely specify a register.
- R0x<3 digit hex address>
  Example: 0x106 —Mode control in Page 1 register 0x6; leading digit signifies page number.
- Data Format (Binary) Column Key in the Register Summary tables. The following key is used to indicate data format:
  ? = Read Only
  d = Read/Write
  0 = Reserved; read 0; must write 0
  1 = Reserved; read 1; must write 1
  r = Reserved; must write back value read
- The following key is used to indicate default value
  X = Indeterminate Register Default Values

Register Definition Table

The register definition tables contain the power-on default values for the bit fields and registers of the MT9M112. Modifying these values may [affect or degrade] the performance of the MT9M112. See the individual register descriptions for more detail.

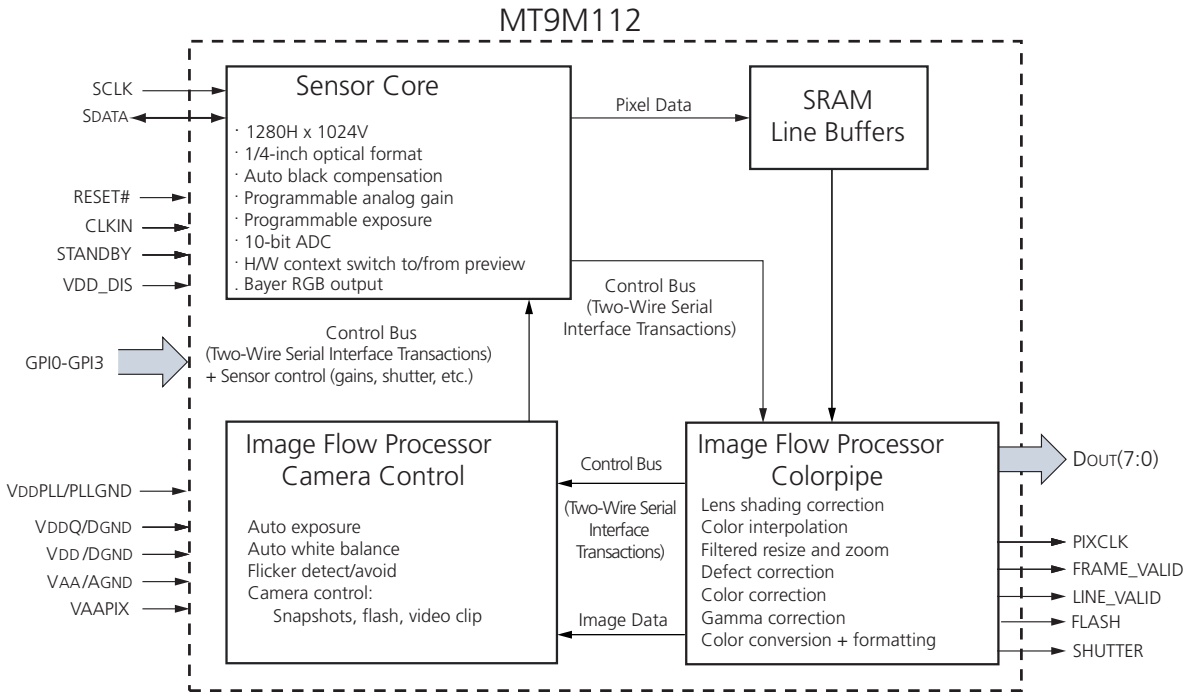
Reserved Registers

Do not alter the reserved registers. If some bits or bit patterns (that is, bit field values) in a register are reserved, they cannot be used. Do not set bit fields to reserved or undefined bit patterns as Micron will not guarantee operation.

The sensor registers are summarized in Table 12 on page 22. The colorpipe registers are summarized in Table 13 on page 26. The camera control registers are summarized in Table 14 on page 29.

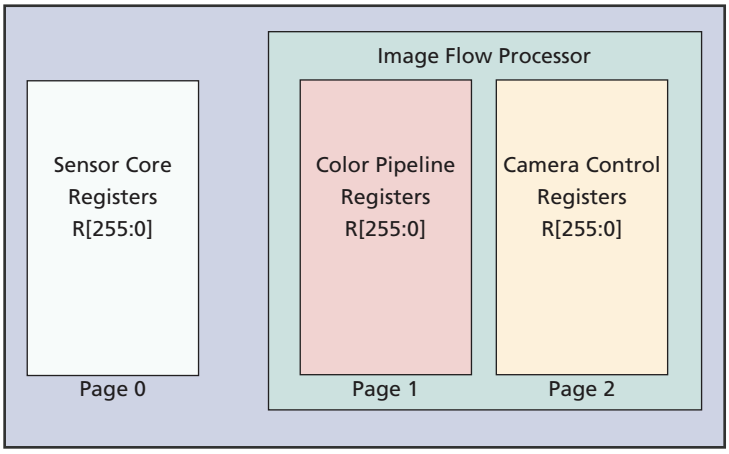
Detailed register descriptions are given in Table 15 on page 33, Table 16 on page 48, and Table 17 on page 64.

Figure 1: Functional Block Diagram



Note: Each of the general purpose input only signals (GPI0–GPI3) must be connected to either DGND or VDDQ for low-power consumption and reliable operation

Figure 2: Internal Registers Grouping



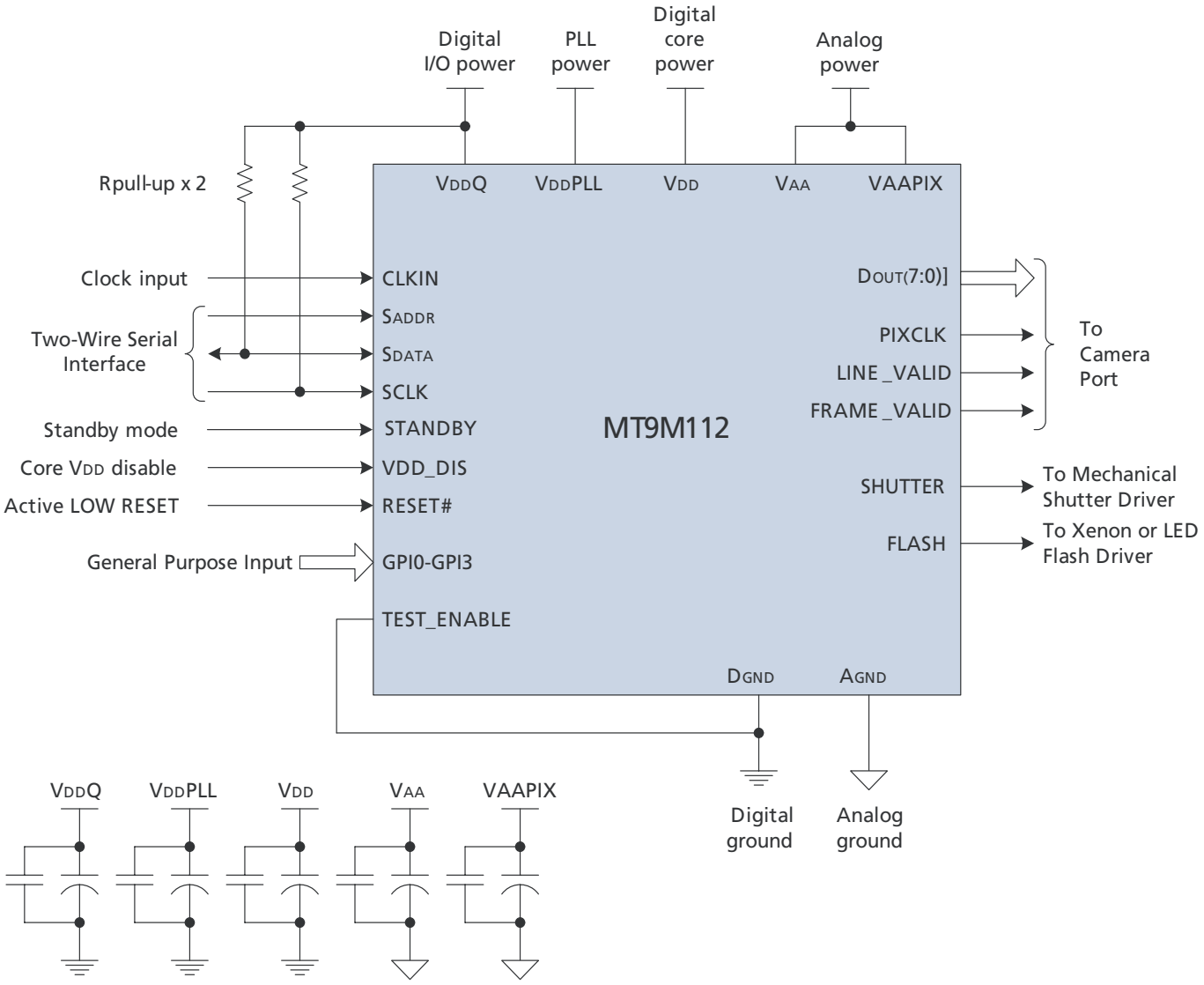
Note: Internal registers are grouped in three address spaces. Register R0xF0 (R240) in each page selects the desired address space.

Typical Connections

Figure 3 shows typical MT9M112 device connections. For low-noise operation, the MT9M112 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails must be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9M112 also supports different digital core (VDD/DGND) and I/O power (VDDQ/DGND) power domains that can be at different voltages. PLL requires a clean power source (VDDPLL).

Figure 3: Typical Configuration (Connection)



Notes: 1. 1. A 1.5KΩ resistor value is recommended for the two-wire serial interface $R_{pull-up}$; however, greater values may be used for slower transmission speeds.
2. MT9M112 STANDBY can be connected to the customer's ASIC controller directly, or to digital GND, depending on the capability of the controller.
3. The PLL bypass capacitor should be connected to VDDPLL and DGND.

Signal Descriptions: Inputs, Outputs and Supply

Table 3: Signal Description

Name	Type	Supply Reference	Description
CLKIN	Input	VDDQ/DGND	Master clock in sensor.
RESET#	Input	VDDQ/DGND	Active LOW: asynchronous reset.
SADDR	Input	VDDQ/DGND	Two-wire serial interface device ID selection 1:0xBA, 0:0x90.
TEST_ENABLE	Input	VDDQ/DGND	Tie to DGND for normal operation (manufacturing use only).
SCLK	Input	VDDQ/DGND	Two-wire serial interface clock.
STANDBY	Input	VDDQ/DGND	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).
VDD_DIS	Input	VDDQ/DGND	Disable core digital VDD for low power operation.
GPI0-GPI3	Input	VDDQ/DGND	General purpose Inputs, do not leave floating; must terminate to either VDDQ or DGND.
SDATA	Bidirectional	VDDQ/DGND	Two-wire serial interface data I/O.
DOUT7-DOUT0	Output	VDDQ/DGND	In normal mode, pixel data output: DOUT7 is the most significant bit (MSB), DOUT0 is the least significant bit (LSB). In 10-bit, SOC bypass mode, DOUT0 is bit 2, DOUTLSB1 is bit 1, and DOUTLSB0 is bit 0.
DOUTLSB1, DOUTLSB0	Output	VDDQ/DGND	Data out bit 1 and 0 in 10-bit SOC bypass mode.
FRAME_VALID	Output	VDDQ/DGND	Active HIGH: FRAME_VALID; indicates active frame.
LINE_VALID	Output	VDDQ/DGND	Active HIGH: LINE_VALID; indicates active pixel.
PIXCLK	Output	VDDQ/DGND	Pixel clock output.
FLASH	Output	VDDQ/DGND	Active HIGH: control external SHUTTER signal (Xenon) or turn on (LED) flash.
SHUTTER	Output	VDDQ/DGND	Active HIGH: controls external mechanical shutter.
AGND	Supply	VAA, VAAPIX	Analog ground.
DGND	Supply	VDD, VDDQ	Common digital core ground and digital I/O ground.
VAA	Supply	AGND	Analog power.
VAAPIX	Supply	AGND	Pixel array analog power supply.
VDD	Supply	DGND	Core digital power.
VDDQ	Supply	DGND	I/O digital power.
VDDPLL	Supply	DGND	PLL power.
DNU	–	–	Factory test signal. Do not connect.

All inputs and outputs are implemented with bidirectional buffers. Care must be taken that all inputs are driven to avoid floating nodes.

Refer to the MT9M112 die data sheet (1/4-inch 1.3-Megapixel SOC Digital Image Sensor Die Features) document for pad number information.

General Purpose Inputs

Logic levels of four general purpose inputs GPI0-GPI3 may be read through the two-wire serial interface facilitating packaging identification. These signals must be terminated to either VDDQ or DGND to ensure that they are not floating.

Architecture Overview

The MT9M112 IFP consists of a color processing pipeline and a measurement and control logic block (the camera controller). The stream of raw data from the sensor enters the pipeline and undergoes several transformations. Image stream processing starts with conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens. Next, the data is interpolated to recover missing color components for each pixel. The resulting interpolated RGB data passes through the current color correction matrix (CCM), saturation, and gamma corrections and is formatted for final output.

The measurement and control logic continuously accumulate image brightness and color statistics. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains that are sent to the sensor core through the control ring bus. The camera control unit also automates taking snapshots, flash snapshots, and video clips using a hardware sequencer.

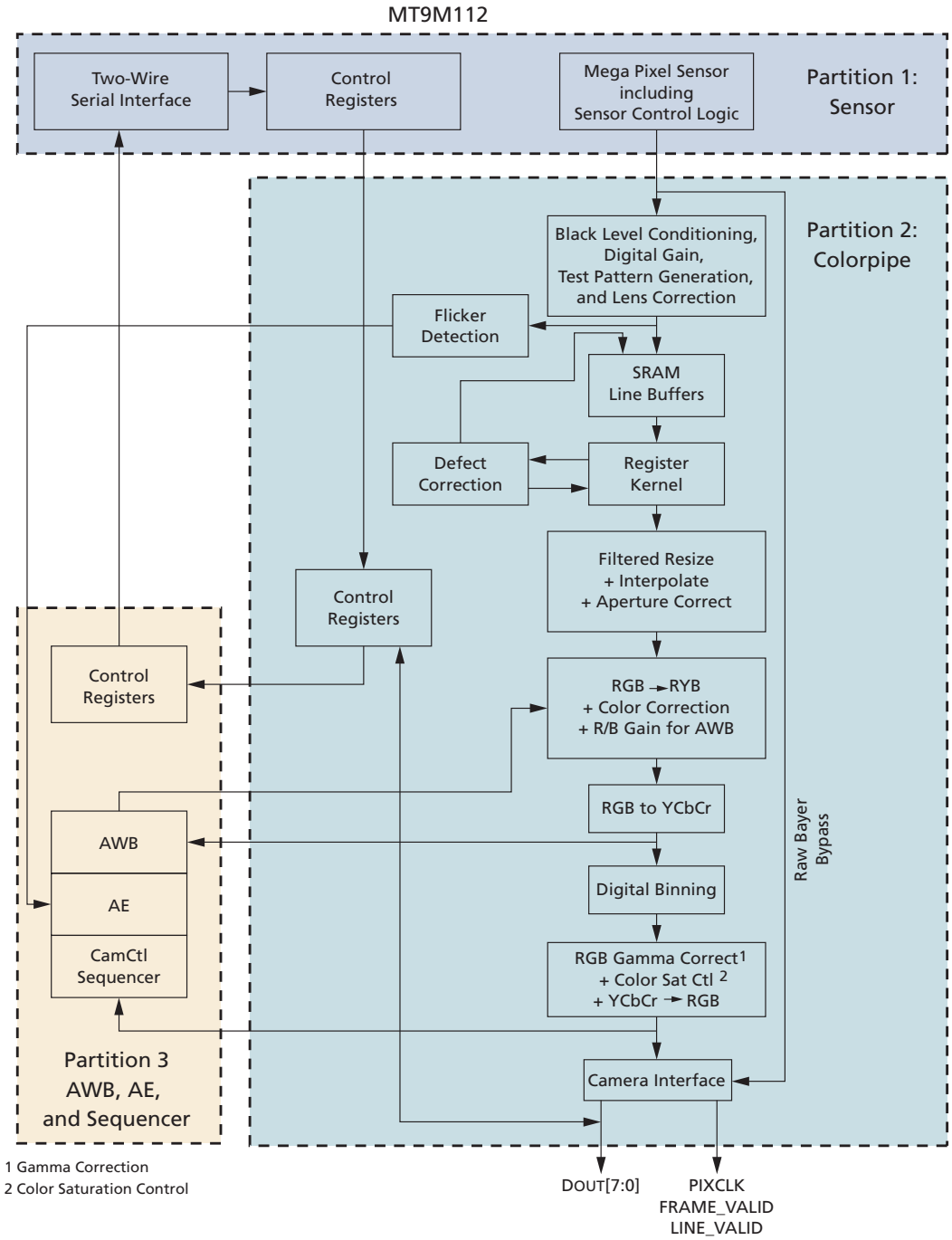
Black Level Conditioning

The sensor core black clamp control works to maintain black pixel values at a constant level, independent of analog gain, reference current, voltage settings, and temperature conditions. If this black level is above zero, it must be reduced before color processing can begin. The black level subtraction block remaps the black level, or pedestal, of the sensor to zero prior to lens shading correction. Following lens shading correction, the black level addition block provides capability for another black level adjustment. However, for good contrast, this level should be set to zero.

Digital Gain and Test Pattern

Controlled by auto exposure logic, the input digital gain stage amplifies the raw image in low-light conditions. A built-in test pattern generator produces a test image stream that can be multiplexed at the output of the gain stage.

Figure 4: IFP Block Diagram



Lens Shading Correction

Inexpensive lenses tend to attenuate image intensity near the edges of pixel arrays. Other factors also cause signal and coloration differences across the image. The net result of all these factors is known as lens shading. Lens shading correction (LC) compensates for these differences.

Typically, the profile of lens shading induced anomalies across the frame is different for each color component. Lens shading correction is independently calibrated for each of the RGB color channels.

The lens shading correction module incorporates a first exposure controlled digital gain, a second auto exposure controlled digital gain, and black level adjustments.

Interpolation, Filtered Resize, and Aperture Correction

A demosaic engine converts the single color per pixel Bayer data from the sensor into 30-bit RGB pixels. The demosaic algorithm analyzes neighboring pixels to generate a best guess for the missing color components. Edge sharpness is preserved as much as possible. Green balance compensation is added to mask the symptoms of green imbalance.

A resize engine uses weighted sampling to smoothly reduce the image by any number of pixels or lines. A digital pixel averaging or binning module extends the reduction range to 10x or more without aliasing. Both reduction engines are set up automatically in hardware so the software driver just has to load the desired output image size and zoom window.

Automatic zoom with single bit zoom-in and zoom-out controls emulates zoom lens behavior. The zoom rate is programmable to optimize zoom response for each application.

Reducer and zoom window changes are synchronized so the reducer and zoom programming do not have to be coordinated with video frame timing. Zoom slow steps the zoom window only on every other frame, allowing auto exposure more time to adapt to each zoom window change.

Aperture correction sharpens the image by an adjustable amount. Sharpening can be programmed to phase out as light levels drop to avoid amplifying noise.

Defect Correction

The MT9M112 has 2D defect correction where pixels with values different from their neighbors by a programmable threshold are considered defects and are replaced.

Color Correction

To obtain good color rendition and saturation, it is necessary to compensate for the differences between the spectral characteristics of the imager color filter array and the spectral response of the human eye. This compensation is achieved through linear transformation of the image with a 3 x 3 element color correction matrix. Optimum values for the color correction coefficients depend on the spectrum of the incident illumination and can either be programmed by the user, or automatically selected by the AWB algorithm described in “Automatic White Balance (AWB)” on page 16.

3-Channel Gamma Correction

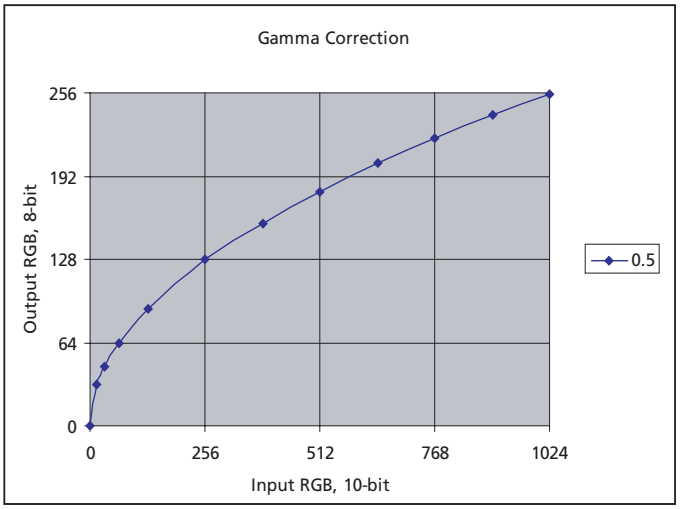
A separate gamma correction function operates on each of the R, G, and B components of the image and enables compensation for nonlinear dependence of the display device output versus driving signal (for example, monitor brightness versus CRT voltage).

In addition, gamma correction provides range compression, converting 10-bit R, G, B input to 8-bit output. Pre-gamma image processing generates 10-bit R, G, B values ranging from 0 to 1024 inclusive. Piecewise linear gamma correction utilized in this imager has eleven intervals, with end points corresponding to the following input values:

$X_I = 0…11 = \{0,16,32,64,128,256,384,512,640,768,896,1024\}$

For each input value X_I, the user can program the corresponding output value Y_I. Y_I values which must be non-decreasing. The MT9M112 supports two context-switchable gamma tables.

Figure 5: Gamma Correction Curve



Color Saturation Control

The MT9M112 supports gradual color saturation reduction in the brightest areas of the image, helping eliminate color artifacts related to clipped pixel values. For noise reduction, both color saturation and sharpness enhancement can be set by the user or adjusted automatically by tracking the magnitude of the gains used by the auto exposure algorithm. Color saturation may be scaled by a constant value of either 0 percent (black and white), 25 percent (1/4), 37.5 percent (3/8), 50 percent (1/2), 75 percent (3/4), 100 percent (1/1), 112.5 percent (9/8), 125 percent (5/4), 137.5 percent (11/8), and 150 percent (3/2).

ITU-R BT.656 and RGB Output

The MT9M112 outputs processed video as a standard ITU-R BT.656 stream, an RGB stream, or as processed or unprocessed Bayer data. The ITU-R BT.656 stream contains YCbCr 4:2:2 data with optional embedded synchronization codes. This output is typically suitable for subsequent display by standard video equipment or JPEG/MPEG compression. RGB functionality provides support for LCD devices.

The MT9M112 can be configured to output 16-bit RGB (RGB565), 15-bit RGB (RGB555), and two types of 12-bit RGB (RGB444). The user can configure internal registers to swap odd and even bytes, chrominance channels, and luminance and chrominance components to interface with application processors. Refer to Table 4 on page 19 through Table 11 on page 20 for more details.

Details of Bayer Output

Unprocessed Bayer data is generated when bypassing the SOC IFP completely. The raw sensor Bayer data stream can be timed using FRAME_VALID, LINE_VALID, and PIXCLK.

In processed Bayer mode, processed RGB is resampled to reduce the data rate by half. Each internal RGB pixel is converted to the 8-bit value of one of the colors: R, G, or B. The pixel pattern is the same as conventional Bayer data, for example GRGR… on one line followed by BGBG… on the next. The receiver interpolates the pixel data to recover the automatically exposed and white balanced image data.

Additional Output Timing Formats

In addition to the color formats detailed above, the MT9M112 supports a number of output timing formats.

Standard: This format includes standard data output, FRAME_VALID, LINE_VALID, and pixel clock signaling. The pixel clock runs continuously, but is gated high for invalid pixel values occurring during an active line. Pixel clock gating occurs when the pixel rate is less than the maximum allowed by the clock—this is typical during preview mode or output image resizing.

ITU-R BT.656: ITU-R BT.656 with synchronization codes. Pixel data is again timed with pixel clock, but FRAME_VALID and LINE_VALID are exchanged for synchronization codes embedded in the pixel stream.

Inactive Pixel Clock: A variant on the standard format, where the pixel clock is gated inactive during both horizontal blanking and vertical blanking.

Automatic White Balance (AWB)

The MT9M112 has a built-in AWB algorithm designed to compensate for the effects of changing scene illumination on the quality of the color rendition. This sophisticated algorithm consists of three major submodules:

- A measurement engine (ME) performing statistical analysis of the image.
- A module selecting the optimal color correction matrix and analog color channel gains in the sensor core.
- A color channel gain control module that fine tunes the color correction matrix and determines the digital gains in the colorpipe.

While the default algorithm settings are adequate in most situations, the user can reprogram base and delta color correction matrices, limit color channel gains, and control the speed of both matrix and gain adjustments. The AWB does not attempt to locate the brightest or grayest elements in the image; it performs in-depth image analysis to differentiate between changes in predominant spectra of illumination and changes in predominant scene colors. Factory defaults are suitable for most applications. However, a wide range of algorithm parameters can be overwritten by the user through the serial interface.

The MT9M112 includes specific, dedicated support for flash photography by means of a flash color correction matrix position. The matrix at the flash matrix position matches the illumination characteristics of the desired LED or Xenon flash. In concert with the auto exposure unit, a decision is made during the sequencing of the flash snapshot as to whether to use the flash matrix (for example, for LEDs, where the flash matrix is only used when it is known if the scene illumination changed significantly).

Auto Exposure

The auto exposure algorithm performs automatic adjustments to image brightness by controlling exposure time and analog gains in the sensor core, as well as digital gain applied to the image. The algorithm relies on the auto exposure measurement engine that tracks speed and amplitude changes in the overall luminance of selected windows in the image. Backlight compensation is achieved by weighting the luminance in the center of the image higher than the luminance on the periphery. Other algorithm features include fast-fluctuating illumination rejection (time averaging), response-speed control, and controlled sensitivity to small changes. While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters, as described above. The auto exposure algorithm enables compensation for a broad range of illumination intensities, with overall range-of-adjustment better than 192,000:1.

The MT9M112 introduces a new auto exposure algorithm that uses a dynamically varying luma target. Alternatively, this algorithm can be turned off and classic auto exposure would take effect.

The MT9M112 also includes fast adaptation modes that are key for LED flash adaptation where convergence within three frames is critical. These modes are used only with classic auto exposure, which is the recommended option when operating flash.

Adaptation mode selection is context-switchable—for example, slower mode for preview video and fast adaptation for flash snapshots. See Contexts and Context Switching below.

Automatic Flicker Detection

Flicker occurs when integration time is not an integer multiple of the period of the light intensity. Automatic flicker detection block does not compensate for the flicker; it reduces flicker occurrence by detecting flicker frequency and adjusting the integration time. For integration times shorter than the light intensity period (10ms for 50Hz environments and 8.33ms for 60Hz environments), flicker is unavoidable.

Flash Light Control

The MT9M112 supports both LED and Xenon-type flash light sources using a dedicated output signal. For Xenon devices, the signal generates a SHUTTER signal to fire when the imager shutter is fully open. For LED, the signal can be asserted or deasserted asynchronously. Flash modes can be configured and engaged over the two-wire serial interface. The flash can be fired either under user control through the two-wire serial interface or by the camera control sequencer. Up to 256 snapshot frames can be captured after the flash is triggered.

Contexts and Context Switching

For a number of parameters in the MT9M112, registers for the storage of two contexts are provided—context A and context B. This enables the user to set up the camera for a number of different modes and then switch between them with a single register write to one of two context control registers (CCRs). Each bit in a CCR typically controls the context of one parameter. Examples of context-switchable parameters include zoom and resize settings, auto exposure speed and algorithm selection, gamma correction table, and output format. Arming a Xenon flash and turning an LED on or off are also considered contexts.

Camera Control Sequencer

Working in concert with the context-switching mechanism, the camera control sequencer automates the process of taking snapshots, flash snapshots, and video clips. The sequencer cycles the camera through a number of different modes, one per frame, switching appropriate parameter contexts each time. For example, to take an LED snapshot, proceed as follows:

Frame 0:

Prior to sequence start, the sensor is in preview mode. The resize unit is set up for a small LCD; the LED is off and auto exposure is in moderate or slow adaptation, as suitable for the preview function or streaming video.

Frame 1:

The sequencer is instructed to take an LED flash snapshot and begins the LED flash snapshot program sequence: The LED is turned on, the resize unit is switched to snapshot resolution settings, auto exposure is switched to fast adaptation and instructed to calculate the delta luma, which is the difference in scene luminance between when the LED is off and when the LED is on.

The magnitude of the change is the basis for deciding if a flash matrix (a color correction matrix at a position optimized for the LED spectrum) needs to be loaded. The output image frame is optionally blanked by extending vertical blanking if the host only wants to receive frames with color correction applied.

Frame 2:

Decision frame: if the delta luma value is sufficiently great, the flash AWB state is loaded. Auto exposure continues to adapt, and again the output image frame is optionally blanked. The LED remains on.

Frame 3:

Snapshot frame: the LED remains on and snapshot image frame is output.

Frame 4:

Return to preview mode: The sequencer restores the state of the resize and output format contents to its preview mode settings. The LED is turned off.

The sequencer provides a mechanism with limited configuration options for typical snapshot and video-clip sequences in its fully automatic operating mode. This mechanism makes it very simple to take good quality pictures and video clips. However, the sequencer can be completely overridden; all context-switching and parameter-update timing mechanisms are made fully available to the driver in semi-automatic mode. Even more flexible parameter update timing control is available in the fully manual mode; however, the driver has to then explicitly maintain timing relationships with events such as the onset of vertical blanking.

Output Data Ordering

The following tables describe the output data order depending on the mode selected.

Table 4: Data Ordering in YCbCr Mode

Mode	Byte	Byte+1	Byte+2	Byte+3
Default	Cb_i	Y_i	Cr_i	Y_{i+1}
Swap Red and Blue	Cr_i	Y_i	Cb_i	Y_{i+1}
Swap bytes	Y_i	Cb_i	Y_{i+1}	Cr_i
Swap Red and Blue, Swap bytes	Y_i	Cr_i	Y_{i+1}	Cb_i

Table 5: Output Data Ordering in Processed Bayer Mode

Mode	Line	Byte	Byte+1	Byte+2	Byte+3
Default	First	G_i	R_{i+1}	G_{i+2}	R_{i+3}
	Second	B_i	G_{i+1}	B_{i+2}	G_{i+3}
Flip Bayer column	First	R_i	G_{i+1}	R_{i+2}	G_{i+3}
	Second	G_i	B_{i+1}	G_{i+2}	B_{i+3}
Flip Bayer row	First	B_i	G_{i+1}	B_{i+2}	G_{i+3}
	Second	G_i	R_{i+1}	G_{i+2}	R_{i+3}
Flip Bayer column Flip Bayer row	First	G_i	B_{i+1}	G_{i+2}	B_{i+3}
	Second	R_i	G_{i+1}	R_{i+2}	G_{i+3}

Table 6: Output Data Ordering in RGB Mode

Mode (Swap disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
RGB565	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
RGB555	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
RGB444x	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
RGBx444	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Table 7: Output Data Ordering in (8 + 2) Bypass Mode

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
8 + 2 bypass	First	B9	B8	B7	B6	B5	B4	B3	B2
	Second	0	0	0	0	0	0	B1	B0

Table 8: Bayer Output Order R0x108[1:0] = 00

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
0	0	First	G	R	G	R
		Second	B	G	B	G

Table 9: Bayer Output Order R0x108[1:0] = 01

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
0	1	First	R	G	R	G
		Second	G	B	G	B

Table 10: Bayer Output Order R0x108[1:0] = 10

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
1	0	First	B	G	B	G
		Second	G	R	G	R

Table 11: Bayer Output Order R0x108[1:0] = 11

R0x108[1] Vertical	R0x108[0] Horizontal		Column			
		Row	1st	2nd	3rd	4th
1	1	First	G	B	G	B
		Second	R	G	R	G

MT9M112 Registers

Double-Buffered Registers

Some sensor settings cannot be changed during frame readout. For example, changing row width R0x003 part way through frame readout results in inconsistent LINE_VALID behavior. To avoid this, the MT9M112 double-buffers many registers by implementing a pending and a live version. Reads and writes access the pending register; the live register controls the sensor operation.

The value in the pending register is transferred to a live register at a fixed point in the frame timing called frame start. Frame start is defined as the point at which the first dark row is read out. By default, this occurs ten row times before FRAME_VALID goes high. R0x022 enables the dark rows to be shown in the image, but this has no effect on the position of frame start.

To determine which registers or register fields are double-buffered in this way, see the synd'c-to-frame start column in Table 15 on page 33.

R0x00D[15] can be used to inhibit transfers from the pending to the live registers. Use this control bit when making many register changes that must take effect simultaneously.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time, or where offsets to the pixel values changed during the frame.

Many changes to the sensor register settings can cause a bad frame. For example, when row width R0x003 is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start has been integrated using the old row width. Consequently, reading it out using the new row width results in a frame with an incorrect integration time.

By default, most bad frames are masked: LINE_VALID and FRAME_VALID are inhibited for these frames, so that the vertical blanking time between frames is extended by the frame time.

To determine which register or register field changes can produce a bad frame, see Table 15 on page 33, the bad frame column, and these notations:

- N—No. Changing the register value does not produce a bad frame.
- Y—Yes. Changing the register value might produce a bad frame.
- YM—Yes; but the bad frame is masked out unless the show bad frames feature (R0x00D[8])is enabled.

Sensor Core Registers – Summary

Register addresses that do not appear in the summary tables are not used by the MT9M112. A summary of the sensor core registers is shown in Table 12.

Table 12: Page 0: Sensor Core Register Summary

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Sensor Core Registers	Data Format (Binary)	Default Value Decimal (Hex)
R0:0 (R0x000)	Chip Version	???? ???? ???? ????	5260 (0x148C)
R1:0 (R0x001)	Row Start	0000 0ddd dddd dddd	28 (0x001C)
R2:0 (R0x002)	Column Start	0000 0ddd dddd dddd	104 (0x0068)
R3:0 (R0x003)	Row Width	0000 0ddd dddd dddd	1024 (0x0400)
R4:0 (R0x004)	Column Width	0000 0ddd dddd dddd	1280 (0x0500)
R5:0 (R0x005)	Horizontal Blanking-Context B	00dd dddd dddd dddd	280 (0x0118)
R6:0 (R0x006)	Vertical Blanking-Context B	0ddd dddd dddd dddd	13 (0x000D)
R7:0 (R0x007)	Horizontal Blanking-Context A	00dd dddd dddd dddd	192 (0x00C0)
R8:0 (R0x008)	Vertical Blanking-Context A	0ddd dddd dddd dddd	9 (0x0009)
R9:0 (R0x009)	Shutter Width	dddd dddd dddd dddd	476 (0x01DC)
R10:0 (R0x00A)	Row Speed	ddd0 000d dddd dddd	32785 (0x8011)
R11:0 (R0x00B)	Extra Delay	00dd dddd dddd dddd	0 (0x0000)
R12:0 (R0x00C)	Shutter Delay	00dd dddd dddd dddd	0 (0x0000)
R13:0 (R0x00D)	Reset	d0d0 0ddd dddd dddd	8 (0x0008)
R31:0 (R0x01F)	FRAME_VALID Control	dddd dddd dddd dddd	0 (0x0000)
R32:0 (R0x020)	Read Mode-Context B	d0dd dd0d dddd dddd	256 (0x0100)
R33:0 (R0x021)	Read Mode-Context A	d000 0d00 dddd dd00	33792 (0x8400)
R34:0 (R0x022)	Dark Columns/Rows	0000 dddd dddd dddd	3343 (0x0D0F)
R35:0 (R0x023)	Flash Control	??dd dddd dddd dddd	3592 (0x0E08)
R36:0 (R0x024)	Extra Reset	dd?? ???? ???? ????	32768 (0x8000)
R37:0 (R0x025)	LINE_VALID Control	dd00 0000 0000 0000	0 (0x0000)
R43:0 (R0x02B)	Green1 Gain	0ddd dddd dddd dddd	32 (0x0020)
R44:0 (R0x02C)	Blue Gain	0ddd dddd dddd dddd	32 (0x0020)
R45:0 (R0x02D)	Red Gain	0ddd dddd dddd dddd	32 (0x0020)
R46:0 (R0x02E)	Green2 Gain	0ddd dddd dddd dddd	32 (0x0020)
R47:0 (R0x02F)	Global Gain	dddd dddd dddd dddd	32 (0x0020)
R48:0 (R0x030)	Row Noise	0ddd dddd dddd dddd	1066 (0x042A)
R49:0 (R0x031)	Reserved	–	7168 (0x1C00)
R50:0 (R0x032)	Reserved	–	0 (0x0000)
R51:0 (R0x033)	Reserved	–	771 (0x0303)
R52:0 (R0x034)	Reserved	–	2061 (0x080D)
R53:0 (R0x035)	Reserved	–	37 (0x0025)
R56:0 (R0x038)	Reserved	–	40965 (0xA005)
R57:0 (R0x039)	Reserved	–	68 (0x0044)
R58:0 (R0x03A)	Reserved	–	8320 (0x2080)
R59:0 (R0x03B)	Reserved	–	32 (0x0020)
R60:0 (R0x03C)	Reserved	–	6688 (0x1A20)
R61:0 (R0x03D)	Reserved	–	8224 (0x2020)
R62:0 (R0x03E)	Reserved	–	8224 (0x2020)

Table 12: Page 0: Sensor Core Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Sensor Core Registers	Data Format (Binary)	Default Value Decimal (Hex)
R63:0 (R0x03F)	Reserved	–	8192 (0x2000)
R64:0 (R0x040)	Reserved	–	26 (0x001A)
R65:0 (R0x041)	Reserved	–	216 (0x00D8)
R66:0 (R0x042)	Reserved	–	34956 (0x888C)
R67:0 (R0x043)	Reserved	–	33667 (0x8383)
R74:0 (R0x04A)	Reserved	–	3344 (0x0D10)
R75:0 (R0x04B)	Reserved	–	4096 (0x1000)
R76:0 (R0x04C)	Reserved	–	13 (0x000D)
R86:0 (R0x056)	Reserved	–	34815 (0x87FF)
R87:0 (R0x057)	Reserved	–	2 (0x0002)
R88:0 (R0x058)	Reserved	–	0 (0x0000)
R89:0 (R0x059)	Black rows	0000 0000 dddd dddd	255 (0x00FF)
R90:0 (R0x05A)	Reserved	–	57354 (0xE00A)
R91:0 (R0x05B)	Dark Green1 Average	0000 0000 0??? ????	0 (0x0000)
R92:0 (R0x05C)	Dark Blue Average	0000 0000 0??? ????	0 (0x0000)
R93:0 (R0x05D)	Dark Red Average	0000 0000 0??? ????	0 (0x0000)
R94:0 (R0x05E)	Dark Green2 Average	0000 0000 0??? ????	0 (0x0000)
R95:0 (R0x05F)	Calibration Threshold	0ddd dddd 0ddd dddd	8989 (0x231D)
R96:0 (R0x060)	Calibration Control	d00d 0ddd dddd dddd	128 (0x0080)
R97:0 (R0x061)	Calibration Green1	0000 000d dddd dddd	0 (0x0000)
R98:0 (R0x062)	Calibration Blue	0000 000d dddd dddd	0 (0x0000)
R99:0 (R0x063)	Calibration Red	0000 000d dddd dddd	0 (0x0000)
R100:0 (R0x064)	Calibration Green2	0000 000d dddd dddd	0 (0x0000)
R101:0 (R0x065)	Clock Control	dddd d000 0000 dddd	57344 (0xE000)
R102:0 (R0x066)	PLL control 1	dddd dddd 00dd dddd	7681 (0x1E01)
R103:0 (R0x067)	PLL control 2	0000 dddd 0ddd dddd	1281 (0x0501)
R104:0 (R0x068)	IO Slew Rate Control	0000 0000 0ddd dddd	93 (0x005D)
R105:0 (R0x069)	Reserved	–	33280 (0x8200)
R106:0 (R0x06A)	Reserved	–	519 (0x0207)
R107:0 (R0x06B)	Reserved	–	33793 (0x8401)
R108:0 (R0x06C)	Reserved	–	32565 (0x7F35)
R109:0 (R0x06D)	Reserved	–	12808 (0x3208)
R110:0 (R0x06E)	Reserved	–	4100 (0x1004)
R111:0 (R0x06F)	Reserved	–	22322 (0x5732)
R112:0 (R0x070)	Reserved	–	33026 (0x8102)
R113:0 (R0x071)	Reserved	–	33025 (0x8101)
R114:0 (R0x072)	Reserved	–	4100 (0x1004)
R115:0 (R0x073)	Reserved	–	3845 (0x0F05)
R116:0 (R0x074)	Reserved	–	22322 (0x5732)
R117:0 (R0x075)	Reserved	–	22067 (0x5633)
R118:0 (R0x076)	Reserved	–	32309 (0x7E35)
R119:0 (R0x077)	Reserved	–	12552 (0x3108)
R120:0 (R0x078)	Reserved	–	33793 (0x8401)
R121:0 (R0x079)	Reserved	–	32514 (0x7F02)

Table 12: Page 0: Sensor Core Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Sensor Core Registers	Data Format (Binary)	Default Value Decimal (Hex)
R122:0 (R0x07A)	Reserved	–	32782 (0x800E)
R123:0 (R0x07B)	Reserved	–	35329 (0x8A01)
R124:0 (R0x07C)	Reserved	–	33281 (0x8201)
R125:0 (R0x07D)	Reserved	–	12806 (0x3206)
R126:0 (R0x07E)	Reserved	–	138 (0x008A)
R127:0 (R0x07F)	Reserved	–	32782 (0x800E)
R130:0 (R0x082)	Reserved	–	24835 (0x6103)
R131:0 (R0x083)	Reserved	–	24597 (0x6015)
R132:0 (R0x084)	Reserved	–	20997 (0x5205)
R133:0 (R0x085)	Reserved	–	20763 (0x511B)
R134:0 (R0x086)	Reserved	–	26113 (0x6601)
R135:0 (R0x087)	Reserved	–	103 (0x0067)
R136:0 (R0x088)	Reserved	–	21251 (0x5303)
R137:0 (R0x089)	Reserved	–	25089 (0x6201)
R138:0 (R0x08A)	Reserved	–	33026 (0x8102)
R139:0 (R0x08B)	Reserved	–	32771 (0x8003)
R140:0 (R0x08C)	Reserved	–	32771 (0x8003)
R141:0 (R0x08D)	Reserved	–	12552 (0x3108)
R142:0 (R0x08E)	Reserved	–	32514 (0x7F02)
R143:0 (R0x08F)	Reserved	–	32514 (0x7F02)
R144:0 (R0x090)	Reserved	–	255 (0x00FF)
R146:0 (R0x092)	Reserved	–	22067 (0x5633)
R149:0 (R0x095)	Reserved	–	255 (0x00FF)
R151:0 (R0x097)	Reserved	–	3845 (0x0F05)
R154:0 (R0x09A)	Reserved	–	255 (0x00FF)
R155:0 (R0x09B)	Reserved	–	255 (0x00FF)
R156:0 (R0x09C)	Reserved	–	255 (0x00FF)
R157:0 (R0x09D)	Reserved	–	34691 (0x8783)
R158:0 (R0x09E)	Reserved	–	255 (0x00FF)
R159:0 (R0x09F)	Reserved	–	255 (0x00FF)
R160:0 (R0x0A0)	Reserved	–	127 (0x007F)
R162:0 (R0x0A2)	Reserved	–	20763 (0x511B)
R165:0 (R0x0A5)	Reserved	–	127 (0x007F)
R167:0 (R0x0A7)	Reserved	–	24597 (0x6015)
R170:0 (R0x0AA)	Reserved	–	255 (0x00FF)
R172:0 (R0x0AC)	Reserved	–	35329 (0x8A01)
R173:0 (R0x0AD)	Reserved	–	33025 (0x8101)
R174:0 (R0x0AE)	Reserved	–	33026 (0x8102)
R176:0 (R0x0B0)	Reserved	–	5120 (0x1400)
R177:0 (R0x0B1)	Reserved	–	4865 (0x1301)
R178:0 (R0x0B2)	Reserved	–	4610 (0x1202)
R179:0 (R0x0B3)	Reserved	–	5120 (0x1400)
R180:0 (R0x0B4)	Reserved	–	4865 (0x1301)
R181:0 (R0x0B5)	Reserved	–	4610 (0x1202)

Table 12: Page 0: Sensor Core Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Sensor Core Registers	Data Format (Binary)	Default Value Decimal (Hex)
R182:0 (R0x0B6)	Reserved	–	34 (0x0022)
R183:0 (R0x0B7)	Reserved	–	20 (0x0014)
R187:0 (R0x0BB)	Reserved	–	255 (0x00FF)
R188:0 (R0x0BC)	Reserved	–	127 (0x007F)
R189:0 (R0x0BD)	Reserved	–	127 (0x007F)
R190:0 (R0x0BE)	Reserved	–	255 (0x00FF)
R191:0 (R0x0BF)	Reserved	–	127 (0x007F)
R192:0 (R0x0C0)	Global Shutter Control	d000 0000 0000 0ddd	0 (0x0000)
R193:0 (R0x0C1)	Start Integration (0xT1)	dddd dddd dddd dddd	75 (0x004B)
R194:0 (R0x0C2)	Start Readout (0xT2)	dddd dddd dddd dddd	75 (0x004B)
R195:0 (R0x0C3)	Assert SHUTTER signal (0xT3)	dddd dddd dddd dddd	113 (0x0071)
R196:0 (R0x0C4)	Deassert SHUTTER signal (0xT4)	dddd dddd dddd dddd	150 (0x0096)
R197:0 (R0x0C5)	Assert flash	dddd dddd dddd dddd	75 (0x004B)
R198:0 (R0x0C6)	Deassert Flash	dddd dddd dddd dddd	90 (0x005A)
R199:0 (R0x0C7)	Reserved	–	15000 (0x3A98)
R200:0 (R0x0C8)	Context Control	d000 0000 d000 dddd	0 (0x0000)
R201:0 (R0x0C9)	Reserved	–	6000 (0x1770)
R202:0 (R0x0CA)	Reserved	–	23 (0x0017)
R203:0 (R0x0CB)	Reserved	–	450 (0x01C2)
R224:0 (R0x0E0)	Reserved	–	0 (0x0000)
R225:0 (R0x0E1)	Reserved	–	0 (0x0000)
R226:0 (R0x0E2)	Reserved	–	0 (0x0000)
R227:0 (R0x0E3)	Reserved	–	0 (0x0000)
R240:0 (R0x0F0)	Page Map	0000 0000 0000 0ddd	0 (0x0000)
R241:0 (R0x0F1)	Byte Wise Address	dddd dddd dddd dddd	0 (0x0000)
R245:0 (R0x0F5)	Reserved	–	2047 (0x07FF)
R246:0 (R0x0F6)	Reserved	–	2047 (0x07FF)
R249:0 (R0x0F9)	Reserved	–	0 (0x0000)
R250:0 (R0x0FA)	Reserved	–	0 (0x0000)
R251:0 (R0x0FB)	Reserved	–	0 (0x0000)
R252:0 (R0x0FC)	Reserved	–	0 (0x0000)
R253:0 (R0x0FD)	Reserved	–	0 (0x0000)
R255:0 (R0x0FF)	Chip Version	???? ???? ???? ????	5260 (0x148C)

Image Flow Processing Registers – Summary

Register addresses that do not appear in the summary tables are not used by the MT9M112. A summary of the Image Flow Processing registers is shown in Table 13.

Table 13: Page 1: Image Flow Processing Register Summary

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Image Flow Processing Registers	Data Format (Binary)	Default Value Decimal (Hex)
R0:1 (R0x100)	Module ID	0000 0000 0000 ????	X
R5:1 (R0x105)	Aperture Correction [sharpening] Gain	0000 0000 0000 dddd	11 (0x000B)
R6:1 (R0x106)	Mode Control	dddd dddd dddd dddd	24590 (0x600E)
R8:1 (R0x108)	Format Control	0000 0ddd dddd dddd	128 (0x0080)
R37:1 (R0x125)	Saturation Adjustment	0000 0000 0ddd dddd	77 (0x004D)
R52:1 (R0x134)	Luma Offset [Brightness Control]	dddd dddd dddd dddd	0 (0x0000)
R53:1 (R0x135)	Clipping Limits for Output Luminance	dddd dddd dddd dddd	65280 (0xFF00)
R58:1 (R0x13A)	Output Format Control [Context A]	0ddd dddd dddd dddd	512 (0x0200)
R59:1 (R0x13B)	IFP Black Level Subtraction pre Lens	0000 0ddd dddd dddd	1066 (0x042A)
R60:1 (R0x13C)	IFP Black Level Addition post Lens	0000 0ddd dddd dddd	1024 (0x0400)
R71:1 (R0x147)	Edge Threshold for Noise Reduction (R/W)	dddd dddd dddd dddd	4144 (0x1030)
R72:1 (R0x148)	Test Pattern Generator	0000 0000 dddd dddd	0 (0x0000)
R83:1 (R0x153)	Gamma Table A Knee Points Y1 Y2	dddd dddd dddd dddd	3588 (0x0E04)
R84:1 (R0x154)	Gamma Table A Knee Points Y3 Y4	dddd dddd dddd dddd	19496 (0x4C28)
R85:1 (R0x155)	Gamma Table A Knee Points Y5 Y6	dddd dddd dddd dddd	38775 (0x9777)
R86:1 (R0x156)	Gamma Table A Knee Points Y7 Y8	dddd dddd dddd dddd	51121 (0xC7B1)
R87:1 (R0x157)	Gamma Table A Knee Points Y9 Y10	dddd dddd dddd dddd	61147 (0xEEDB)
R88:1 (R0x158)	Gamma Table A Knee Points Y0 Y11	dddd dddd dddd dddd	65280 (0xFF00)
R128:1 (R0x180)	Lens Correction Control	0000 0000 000d dddd	X
R129:1 (R0x181)	Lens Vertical Red Knee 0 and Initial Value	dddd dddd dddd dddd	X
R130:1 (R0x182)	Lens Vertical Red Knees 2 and 1	dddd dddd dddd dddd	X
R131:1 (R0x183)	Lens Vertical Red Knees 4 and 3	dddd dddd dddd dddd	X
R132:1 (R0x184)	Lens Vertical Green Knee 0 and Initial Value	dddd dddd dddd dddd	X
R133:1 (R0x185)	Lens Vertical Green Knees 2 and 1	dddd dddd dddd dddd	X
R134:1 (R0x186)	Lens Vertical Green Knees 4 and 3	dddd dddd dddd dddd	X
R135:1 (R0x187)	Lens Vertical Blue Knee 0 and Initial Value	dddd dddd dddd dddd	X
R136:1 (R0x188)	Lens Vertical Blue Knees 2 and 1	dddd dddd dddd dddd	X
R137:1 (R0x189)	Lens Vertical Blue Knees 4 and 3	dddd dddd dddd dddd	X
R138:1 (R0x18A)	Lens Horizontal Red Knee 0 and Initial Value	dddd dddd dddd dddd	X
R139:1 (R0x18B)	Lens Horizontal Red Knees 2 and 1	dddd dddd dddd dddd	X
R140:1 (R0x18C)	Lens Horizontal Red Knees 4 and 3	dddd dddd dddd dddd	X
R141:1 (R0x18D)	Lens Horizontal Red Knee 5	0000 0000 dddd dddd	X
R142:1 (R0x18E)	Lens Horizontal Green Knee 0 and Initial Value	dddd dddd dddd dddd	X
R143:1 (R0x18F)	Lens Horizontal Green Knees 2 and 1	dddd dddd dddd dddd	X
R144:1 (R0x190)	Lens Horizontal Green Knees 4 and 3	dddd dddd dddd dddd	X
R145:1 (R0x191)	Lens Horizontal Green Knee 5	0000 0000 dddd dddd	X
R146:1 (R0x192)	Lens Horizontal Blue Knee 0 and Initial Value	dddd dddd dddd dddd	X
R147:1 (R0x193)	Lens Horizontal Blue Knees 2 and 1	dddd dddd dddd dddd	X

Table 13: Page 1: Image Flow Processing Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Image Flow Processing Registers	Data Format (Binary)	Default Value Decimal (Hex)
R148:1 (R0x194)	Lens Horizontal Blue Knees 4 and 3	dddd dddd dddd dddd	X
R149:1 (R0x195)	Lens Horizontal Blue Knee 5	0000 0000 dddd dddd	X
R153:1 (R0x199)	Line Counter	???? ???? ???? ????	0 (RO)
R154:1 (R0x19A)	Frame Counter	???? ???? ???? ????	0 (RO)
R155:1 (R0x19B)	Output Format Control [Context B]	dddd dddd dddd dddd	512 (0x0200)
R157:1 (R0x19D)	Defect Correction and Noise Reduction Control	rrrr rrrr dddd dddd	15534 (0x3CAE)
R161:1 (R0x1A1)	Horizontal Output Size B	0000 0ddd dddd dddd	1280 (0x0500)
R164:1 (R0x1A4)	Vertical Output Size B	0000 0ddd dddd dddd	1024 (0x0400)
R165:1 (R0x1A5)	Horizontal Pan	0d00 0ddd dddd dddd	16384 (0x4000)
R166:1 (R0x1A6)	Horizontal Zoom	0000 0ddd dddd dddd	1280 (0x0500)
R167:1 (R0x1A7)	Horizontal Output Size A	0000 0ddd dddd dddd	640 (0x0280)
R168:1 (R0x1A8)	Vertical Pan	0d00 0ddd dddd dddd	16384 (0x4000)
R169:1 (R0x1A9)	Vertical Zoom	0000 0ddd dddd dddd	1024 (0x0400)
R170:1 (R0x1AA)	Vertical Output Size A	0000 0ddd dddd dddd	512 (0x0200)
R171:1 (R0x1AB)	Reserved	–	0 (0x0000)
R172:1 (R0x1AC)	Reserved	–	0 (0x0000)
R174:1 (R0x1AE)	Reducer Zoom Step Size	dddd dddd dddd dddd	3081 (0x0C09)
R175:1 (R0x1AF)	Reducer Zoom Control	dddd dddd dddd dddd	0 (0x0000)
R179:1 (R0x1B3)	Reserved	–	2 (0x0002)
R180:1 (R0x1B4)	Reserved	–	32 (0x0020)
R182:1 (R0x1B6)	Lens Vertical Red Knees 6 and 5	dddd dddd dddd dddd	X
R183:1 (R0x1B7)	Lens Vertical Red Knees 8 and 7	dddd dddd dddd dddd	X
R184:1 (R0x1B8)	Lens Vertical Green Knees 6 and 5	dddd dddd dddd dddd	X
R185:1 (R0x1B9)	Lens Vertical Green Knees 8 and 7	dddd dddd dddd dddd	X
R186:1 (R0x1BA)	Lens Vertical Blue Knees 6 and 5	dddd dddd dddd dddd	X
R187:1 (R0x1BB)	Lens Vertical Blue Knees 8 and 7	dddd dddd dddd dddd	X
R188:1 (R0x1BC)	Lens Horizontal Red Knees 7 and 6	dddd dddd dddd dddd	X
R189:1 (R0x1BD)	Lens Horizontal Red Knees 9 and 8	dddd dddd dddd dddd	X
R190:1 (R0x1BE)	Lens Horizontal Red Knee 10	0000 0000 dddd dddd	X
R191:1 (R0x1BF)	Lens Horizontal Green Knees 7 and 6	dddd dddd dddd dddd	X
R192:1 (R0x1C0)	Lens Horizontal Green Knees 9 and 8	dddd dddd dddd dddd	X
R193:1 (R0x1C1)	Lens Horizontal Green Knee 10	0000 0000 dddd dddd	X
R194:1 (R0x1C2)	Lens Horizontal Blue Knees 7 and 6	dddd dddd dddd dddd	X
R195:1 (R0x1C3)	Lens Horizontal Blue Knees 9 and 8	dddd dddd dddd dddd	X
R196:1 (R0x1C4)	Lens Horizontal Blue Knee 10	0000 0000 dddd dddd	X
R200:1 (R0x1C8)	Global Context Control (RO)	???? ???? ???? ????	0 (RO)
R201:1 (R0x1C9)	Reserved	–	0 (0x0000)
R202:1 (R0x1CA)	Reserved	–	0 (0x0000)
R203:1 (R0x1CB)	Reserved	–	0 (0x0000)
R204:1 (R0x1CC)	Reserved	–	0 (0x0000)
R205:1 (R0x1CD)	Reserved	–	0 (0x0000)
R206:1 (R0x1CE)	Reserved	–	0 (0x0000)
R207:1 (R0x1CF)	Reserved	–	0 (0x0000)
R208:1 (R0x1D0)	Reserved	–	0 (0x0000)

Table 13: Page 1: Image Flow Processing Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Image Flow Processing Registers	Data Format (Binary)	Default Value Decimal (Hex)
R220:1 (R0x1DC)	Gamma Table B Knee Points Y1 Y2	dddd dddd dddd dddd	3588 (0x0E04)
R221:1 (R0x1DD)	Gamma Table B Knee Points Y3 Y4	dddd dddd dddd dddd	19496 (0x4C28)
R222:1 (R0x1DE)	Gamma Table B Knee Points Y5 Y6	dddd dddd dddd dddd	38775 (0x9777)
R223:1 (R0x1DF)	Gamma Table B Knee Points Y7 Y8	dddd dddd dddd dddd	51121 (0xC7B1)
R224:1 (R0x1E0)	Gamma Table B Knee Points Y9 Y10	dddd dddd dddd dddd	61147 (0xEEDB)
R225:1 (R0x1E1)	Gamma Table B Knee Points Y0 Y11	dddd dddd dddd dddd	65280 (0xFF00)
R226:1 (R0x1E2)	Effects Mode	dddd dddd 0000 0ddd	28672 (0x7000)
R227:1 (R0x1E3)	Effects Sepia Color	dddd dddd dddd dddd	45091 (0xB023)
R240:1 (R0x1F0)	Page Map	0000 0000 0000 0ddd	0 (0x0000)
R241:1 (R0x1F1)	Byte Wise Address	dddd dddd dddd dddd	0 (0x0000)
R250:1 (R0x1FA)	Reserved	–	0 (0x0000)
R251:1 (R0x1FB)	Reserved	–	0 (0x0000)

Camera Control Registers – Summary

Register addresses that do not appear in the summary tables are not used by the MT9M112. A summary of the Camera Control Processing registers is shown in Table 14.

Table 14: Page 2: Camera Control Register Summary

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Camera Control Registers	Data Format (Binary)	Default Value Decimal (Hex)
R2:2 (R0x202)	Base Matrix Signs	0000 000? ddd? ddd?	238 (0x00EE)
R3:2 (R0x203)	Base Matrix Scale K1- K5	0ddd dddd dddd dddd	10531 (0x2923)
R4:2 (R0x204)	Base Matrix Scale K6 - K9	0000 dddd dddd dddd	1252 (0x04E4)
R6:2 (R0x206)	Mode Control (RO)	???? ???? ???? ????	24590 (0x600E)
R9:2 (R0x209)	Base Matrix Coefficient K1	0000 0000 dddd dddd	208 (0x00D0)
R10:2 (R0x20A)	Base Matrix Coefficient K2	0000 0000 dddd dddd	82 (0x0052)
R11:2 (R0x20B)	Base Matrix Coefficient K3	0000 0000 dddd dddd	4 (0x0004)
R12:2 (R0x20C)	Base Matrix Coefficient K4	0000 0000 dddd dddd	148 (0x0094)
R13:2 (R0x20D)	Base Matrix Coefficient K5	0000 0000 dddd dddd	130 (0x0082)
R14:2 (R0x20E)	Base Matrix Coefficient K6	0000 0000 dddd dddd	63 (0x003F)
R15:2 (R0x20F)	Base Matrix Coefficient K7	0000 0000 dddd dddd	96 (0x0060)
R16:2 (R0x210)	Base Matrix Coefficient K8	0000 0000 dddd dddd	156 (0x009C)
R17:2 (R0x211)	Base Matrix Coefficient K9	0000 0000 dddd dddd	182 (0x00B6)
R18:2 (R0x212)	AWB Position	0000 0000 0??? ????	0 (0x0000)
R19:2 (R0x213)	AWB Red Digital Gain	0000 0000 ???? ????	0 (0x0000)
R20:2 (R0x214)	AWB Blue Digital Gain	0000 0000 ???? ????	0 (0x0000)
R21:2 (R0x215)	Delta Coefficients Signs	0000 000d dddd dddd	201 (0x00C9)
R22:2 (R0x216)	Delta Matrix Coefficient D1	0000 0000 dddd dddd	93 (0x005D)
R23:2 (R0x217)	Delta Matrix Coefficient D2	0000 0000 dddd dddd	156 (0x009C)
R24:2 (R0x218)	Delta Matrix Coefficient D3	0000 0000 dddd dddd	3 (0x0003)
R25:2 (R0x219)	Delta Matrix Coefficient D4	0000 0000 dddd dddd	68 (0x0044)
R26:2 (R0x21A)	Delta Matrix Coefficient D5	0000 0000 dddd dddd	9 (0x0009)
R27:2 (R0x21B)	Delta Matrix Coefficient D6	0000 0000 dddd dddd	80 (0x0050)
R28:2 (R0x21C)	Delta Matrix Coefficient D7	0000 0000 dddd dddd	113 (0x0071)
R29:2 (R0x21D)	Delta Matrix Coefficient D8	0000 0000 dddd dddd	121 (0x0079)
R30:2 (R0x21E)	Delta Matrix Coefficient D9	0000 0000 dddd dddd	99 (0x0063)
R31:2 (R0x21F)	White Balance Cb and Cr Limits	0000 0000 dddd dddd	384 (0x0180)
R32:2 (R0x220)	Luminance Limits for White Balance Statistics	dddd dddd dddd dddd	51220 (0xC814)
R33:2 (R0x221)	Red Blue Gain for Manual White Balance	dddd dddd dddd dddd	32896 (0x8080)
R34:2 (R0x222)	AWB Red Limit	dddd dddd dddd dddd	36992 (0x9080)
R35:2 (R0x223)	AWB Blue Limit	dddd dddd dddd dddd	34936 (0x8878)
R36:2 (R0x224)	Matrix Adjustment Limits	0ddd dddd 0ddd ddd	32512 (0x7F00)
R38:2 (R0x226)	Auto Exposure Full Window Horizontal Boundaries	dddd dddd dddd dddd	32768 (0x8000)
R39:2 (R0x227)	Auto Exposure Full Window Vertical Boundaries	dddd dddd dddd dddd	32776 (0x8008)
R40:2 (R0x228)	AWB Advanced Control	rrrd rrrr 0ddd dddd	59906 (0xEA02)
R41:2 (R0x229)	Wide AWB Gates	dddd dddd dddd dddd	34426 (0x867A)
R42:2 (R0x22A)	Standard Deviation Limits for a Monochrome Zone	dddd dddd dddd dddd	208 (0x00D0)
R43:2 (R0x22B)	Auto Exposure Center Window Horizontal Boundaries	dddd dddd dddd dddd	24608 (0x6020)
R44:2 (R0x22C)	Auto Exposure Center Window Vertical Boundaries	dddd dddd dddd dddd	24608 (0x6020)

Table 14: Page 2: Camera Control Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Camera Control Registers	Data Format (Binary)	Default Value Decimal (Hex)
R45:2 (R0x22D)	Boundaries for White Balance Window	dddd dddd dddd dddd	61600 (0xF0A0)
R46:2 (R0x22E)	Auto Exposure Target and Precision Control	dddd dddd dddd dddd	3140 (0x0C44)
R47:2 (R0x22F)	Auto Exposure Speed and Sensitivity Control A	dddd dddd dddd dddd	37152 (0x9120)
R48:2 (R0x230)	Red White Balance Measurement	0000 0000 ???? ????	0 (0x0000)
R49:2 (R0x231)	Luma White Balance Measurement	0000 0000 ???? ????	0 (0x0000)
R50:2 (R0x232)	Blue White Balance Measurement	0000 0000 ???? ????	0 (0x0000)
R51:2 (R0x233)	Sharpness and Saturation Control	dddd dddd dddd dddd	5230 (0x146E)
R53:2 (R0x235)	Dynamic Target Luma	dddd dddd dddd dddd	45072 (0xB010)
R54:2 (R0x236)	Auto Exposure Gain Limits	dddd dddd dddd dddd	30736 (0x7810)
R55:2 (R0x237)	Auto Exposure Gain Zone Limits	d000 00dd dddd dddd	768 (0x0300)
R56:2 (R0x238)	Auto Exposure Gain Table Range Control	0000 dddd dddd dddd	1088 (0x0440)
R57:2 (R0x239)	Auto Exposure Line Size A	0000 0ddd dddd dddd	1680 (0x0690)
R58:2 (R0x23A)	Auto Exposure Line Size B	0000 0ddd dddd dddd	1574 (0x0626)
R59:2 (R0x23B)	Auto Exposure Shutter Delay Limit A	0000 0ddd dddd dddd	990 (0x03DE)
R60:2 (R0x23C)	Auto Exposure Shutter Delay Limit B	0000 0ddd dddd dddd	1226 (0x04CA)
R61:2 (R0x23D)	Auto Exposure ADC Adjustment Limits	00dd dddd dddd dddd	6365 (0x18DD)
R62:2 (R0x23E)	Gain Threshold for CCM Adjustment	000d dddd dddd dddd	7423 (0x1CFF)
R63:2 (R0x23F)	Auto Exposure Zone Index	0000 0000 000? ????	0 (0x0000)
R70:2 (R0x246)	Auto Exposure Zone 0 Luma Threshold	0000 0000 dddd dddd	0 (0x0000)
R75:2 (R0x24B)	Reserved	–	0 (0x0000)
R76:2 (R0x24C)	Auto Exposure Current Measured Luma	???? ???? ???? ????	0 (0x0000)
R77:2 (R0x24D)	Auto Exposure Time Averaged Luma	0000 0000 ???? ????	0 (0x0000)
R79:2 (R0x24F)	Reserved	–	0 (0x0000)
R87:2 (R0x257)	Shutter Width Basis 60Hz A	0000 dddd dddd dddd	476 (0x01DC)
R88:2 (R0x258)	Shutter Width Basis 50Hz A	0000 dddd dddd dddd	571 (0x023B)
R89:2 (R0x259)	Shutter Width Basis 60Hz B	0000 dddd dddd dddd	508 (0x01FC)
R90:2 (R0x25A)	Shutter Width Basis 50Hz B	0000 dddd dddd dddd	609 (0x0261)
R91:2 (R0x25B)	Flicker Control	?000 0000 00dd dddd	2 (0x0002)
R92:2 (R0x25C)	Search flicker 60Hz	dddd dddd dddd dddd	4364 (0x110C)
R93:2 (R0x25D)	Search flicker 50Hz	dddd dddd dddd dddd	5392 (0x1510)
R94:2 (R0x25E)	Ratios of Imager Gains - Base	dddd dddd dddd dddd	22600 (0x5848)
R95:2 (R0x25F)	Ratios of Imager Gains - Delta	dddd dddd dddd dddd	8225 (0x2021)
R96:2 (R0x260)	Ratios of Imager Gains - Delta Signs	0000 0000 0000 00dd	2 (0x0002)
R97:2 (R0x261)	AWB Analog Gain Ratios Monitor	???? ???? ???? ????	0 (0x0000)
R98:2 (R0x262)	Auto Exposure Digital Gains	dddd dddd dddd dddd	0 (0x0000)
R99:2 (R0x263)	Reserved	–	0 (0x0000)
R100:2 (R0x264)	Reserved	–	24092 (0x5E1C)
R101:2 (R0x265)	Auto Exposure Luma Measurement Offset	0000 00dd dddd dddd	0 (0x0000)
R103:2 (R0x267)	Auto Exposure Digital Gain Limits	dddd dddd dddd dddd	8208 (0x2010)
R106:2 (R0x26A)	Reserved	–	0 (0x0000)
R107:2 (R0x26B)	Reserved	–	0 (0x0000)
R108:2 (R0x26C)	Reserved	–	0 (0x0000)
R109:2 (R0x26D)	Reserved	–	0 (0x0000)
R110:2 (R0x26E)	Reserved	–	0 (0x0000)

Table 14: Page 2: Camera Control Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Camera Control Registers	Data Format (Binary)	Default Value Decimal (Hex)
R111:2 (R0x26F)	Reserved	–	0 (0x0000)
R112:2 (R0x270)	Reserved	–	0 (0x0000)
R113:2 (R0x271)	Reserved	–	0 (0x0000)
R114:2 (R0x272)	Reserved	–	0 (0x0000)
R115:2 (R0x273)	Reserved	–	0 (0x0000)
R116:2 (R0x274)	Reserved	–	0 (0x0000)
R117:2 (R0x275)	Reserved	–	0 (0x0000)
R118:2 (R0x276)	Reserved	–	0 (0x0000)
R119:2 (R0x277)	Reserved	–	0 (0x0000)
R120:2 (R0x278)	Reserved	–	0 (0x0000)
R121:2 (R0x279)	Reserved	–	0 (0x0000)
R122:2 (R0x27A)	Reserved	–	0 (0x0000)
R123:2 (R0x27B)	Reserved	–	0 (0x0000)
R124:2 (R0x27C)	Reserved	–	0 (0x0000)
R125:2 (R0x27D)	Reserved	–	0 (0x0000)
R129:2 (R0x281)	Auto Exposure Day/Night Mode Zones	dddd dddd dddd dddd	33544 (0x8308)
R130:2 (R0x282)	Auto Exposure Gain Zone 1 Deltas	0000 00dd dddd dddd	1020 (0x03FC)
R131:2 (R0x283)	Auto Exposure Gain Zone 2 Deltas	0000 00dd dddd dddd	769 (0x0301)
R132:2 (R0x284)	Auto Exposure Gain Zone 3 Deltas	0000 00dd dddd dddd	193 (0x00C1)
R133:2 (R0x285)	Auto Exposure Gain Zone 4 Deltas	0000 00dd dddd dddd	929 (0x03A1)
R134:2 (R0x286)	Auto Exposure Gain Zone 5 Deltas	0000 00dd dddd dddd	980 (0x03D4)
R135:2 (R0x287)	Auto Exposure Gain Zone 6 Deltas	0000 00dd dddd dddd	983 (0x03D7)
R136:2 (R0x288)	Auto Exposure Gain Zone 7 Deltas	0000 00dd dddd dddd	921 (0x0399)
R137:2 (R0x289)	Auto Exposure Gain Zone 8 Deltas	0000 00dd dddd dddd	1016 (0x03F8)
R138:2 (R0x28A)	Auto Exposure Gain Zone 9 Deltas	0000 00dd dddd dddd	28 (0x001C)
R139:2 (R0x28B)	Auto Exposure Gain Zone 10 Deltas	0000 00dd dddd dddd	957 (0x03BD)
R140:2 (R0x28C)	Auto Exposure Gain Zone 11 Deltas	0000 00dd dddd dddd	987 (0x03DB)
R141:2 (R0x28D)	Auto Exposure Gain Zone 12 Deltas	0000 00dd dddd dddd	957 (0x03BD)
R142:2 (R0x28E)	Auto Exposure Gain Zone 13 Deltas	0000 00dd dddd dddd	1020 (0x03FC)
R143:2 (R0x28F)	Auto Exposure Gain Zone 14 Deltas	0000 00dd dddd dddd	990 (0x03DE)
R144:2 (R0x290)	Auto Exposure Gain Zone 15 Deltas	0000 00dd dddd dddd	990 (0x03DE)
R145:2 (R0x291)	Auto Exposure Gain Zone 16 and 17 Deltas	0000 00dd dddd dddd	990 (0x03DE)
R146:2 (R0x292)	Auto Exposure Gain Zone 18 and 19 Deltas	0000 00dd dddd dddd	990 (0x03DE)
R147:2 (R0x293)	Auto Exposure Gain Zone 20 and 21 Deltas	0000 00dd dddd dddd	31 (0x001F)
R148:2 (R0x294)	Auto Exposure Gain Zone 22 and 23 Deltas	0000 00dd dddd dddd	65 (0x0041)
R149:2 (R0x295)	Auto Exposure Gain Zone 24 Deltas	0000 00dd dddd dddd	867 (0x0363)
R150:2 (R0x296)	Reserved	–	0 (0x0000)
R151:2 (R0x297)	Luma Saturation Monitor	???? ???? ???? ????	0 (0x0000)
R152:2 (R0x298)	Reserved	–	255 (0x00FF)
R153:2 (R0x299)	Reserved	–	1 (0x0001)
R154:2 (R0x29A)	Dynamic Target Luma Monitor	???? 0000 dddd dddd	0 (0x0000)
R155:2 (R0x29B)	Dynamic Target Luma Parameters	dddd dddd dddd dddd	217 (0x00D9)
R156:2 (R0x29C)	Auto Exposure Speed and Sensitivity Control B	dddd dddd dddd dddd	53504 (0xD100)
R157:2 (R0x29D)	Black Alarm Pixel Thresholds	dddd dddd dddd dddd	50442 (0xC50A)

Table 14: Page 2: Camera Control Register Summary (continued)

Data format:? = Read Only; d = Read/Write; 0 = Reserved, read 0, must write 0; 1 = Reserved, read 1, must write 1; r = Reserved, must write back value read. Default value: X = Indeterminate

Register # Decimal (Hex)	Camera Control Registers	Data Format (Binary)	Default Value Decimal (Hex)
R160:2 (R0x2A0)	Auto Exposure Maximum Bright Gain Deltas 1 and 2	0000 00dd dddd dddd	254 (0x00FE)
R161:2 (R0x2A1)	Auto Exposure Maximum Bright Gain Deltas 3 and 4	0000 00dd dddd dddd	100 (0x0064)
R162:2 (R0x2A2)	Auto Exposure Maximum Bright Gain Deltas 5 and 6	0000 00dd dddd dddd	66 (0x0042)
R163:2 (R0x2A3)	Auto Exposure Maximum Bright Gain Deltas 7 and 8	0000 00dd dddd dddd	33 (0x0021)
R164:2 (R0x2A4)	Auto Exposure Maximum Bright Gain Deltas 9 and 10	0000 00dd dddd dddd	33 (0x0021)
R165:2 (R0x2A5)	Auto Exposure Maximum Bright Gain Delta 11	0000 0000 00dd dddd	0 (0x0000)
R180:2 (R0x2B4)	Reserved	–	32 (0x0020)
R198:2 (R0x2C6)	Reserved	–	0 (0x0000)
R199:2 (R0x2C7)	Reserved	–	0 (0x0000)
R200:2 (R0x2C8)	Global Context Control	dddd dddd dddd dddd	0 (0x0000)
R201:2 (R0x2C9)	Camera Context Control	rrrr rrrr ???? ????	0 (0x0000)
R203:2 (R0x2CB)	Program Advance	0000 0000 0000 00dd	0 (0x0000)
R204:2 (R0x2CC)	Program Control	0000 0000 00dd dddd	0 (0x0000)
R205:2 (R0x2CD)	Snapshot Program Configuration	0ddd dddd dddd dddd	8608 (0x21A0)
R206:2 (R0x2CE)	LED Flash Snapshot Program Configuration	dddd dddd dddd dddd	7835 (0x1E9B)
R207:2 (R0x2CF)	Auto Exposure/AWB LED Flash Delta Luma Thresholds	dddd dddd dddd dddd	19018 (0x4A4A)
R208:2 (R0x2D0)	Xenon Flash Configuration	00dd dddd dddd dddd	5773 (0x168D)
R209:2 (R0x2D1)	Video Clip Configuration	0000 0000 dddd dddd	77 (0x004D)
R210:2 (R0x2D2)	Default Program Configuration	0000 0000 dddd dddd	0 (0x0000)
R211:2 (R0x2D3)	User Global Context Control	dddd dddd dddd dddd	0 (0x0000)
R212:2 (R0x2D4)	Xenon Flash Auto Exposure Parameters	0ddd dddd dddd dddd	521 (0x0209)
R213:2 (R0x2D5)	Camera Control Context Control	0000 0000 rddd dddd	0 (0x0000)
R214:2 (R0x2D6)	Number of Capture Frame for Snapshot	0000 0000 dddd dddd	0 (0x0000)
R220:2 (R0x2DC)	Mg-G Thresholds	dddd dddd dddd dddd	4088 (0x0FF8)
R221:2 (R0x2DD)	B-R Thresholds	dddd dddd dddd dddd	3296 (0x0CE0)
R222:2 (R0x2DE)	New Chroma Test Enable	0000 0000 0000 000d	1 (0x0001)
R239:2 (R0x2EF)	AWB Advanced Control 2	0000 0000 00dd dddd	8 (0x0008)
R240:2 (R0x2F0)	Page Map	0000 0000 0000 0ddd	0 (0x0000)
R241:2 (R0x2F1)	Byte Wise Address	dddd dddd dddd dddd	0 (0x0000)
R242:2 (R0x2F2)	AWB Digital Gain Offsets	dddd dddd dddd dddd	0 (0x0000)
R243:2 (R0x2F3)	Reserved	–	0 (0x0000)
R245:2 (R0x2F5)	Manual White Balance Matrix Position	0000 0000 dddd dddd	64 (0x0040)
R246:2 (R0x2F6)	Flash White Balance Position	0000 0000 dddd dddd	127 (0x007F)
R255:2 (R0x2FF)	White Balance Flash Gains	dddd dddd dddd dddd	43136 (0xA880)

Page 0: Sensor Core Register Descriptions

Table 15: Page 0: Sensor Core Register Descriptions
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R0:0 R0x000	15:0	0x148C	Hardwired READ only (RO).		
	Uniquely identifies the chip version.				
R1:0 R0x001	10:0	0x1C	Row Start (RW)	Y	YM
	The first row to be read out, excluding any dark rows that may be read. To window the image down, set this register to the starting Y value. Setting a value less than 20 is not recommended because the dark rows should be read using R0x022.				
R2:0 R0x002	10:0	0x68	Column Start (RW)	Y	YM
	The first column to be read out, excluding dark columns that may be read. To window the image down, set this register to the starting X value. Setting a value below 96 is not recommended because readout of dark columns should be controlled by R0x022.				
R3:0 R0x003	10:0	0x400	Row Width (RW)	Y	YM
	Number of rows in the image to be read out, excluding any dark rows or border rows that may be read. The minimum supported value is 2.				
R4:0 R0x004	10:0	0x500	Column Width (RW)	Y	YM
	Number of columns in the image to be read out, excluding any dark columns or border columns that may be read. The minimum supported value is 20.				
R5:0 R0x005	13:0	0x118	Horizontal Blanking-Context B (RW)	Y	YM
	Number of blank columns in a row when context B is selected (R0x0C8[0] = 1). The extra columns are added at the beginning of a row.				
R6:0 R0x006	14:0	0xD	Vertical Blanking-Context B (RW)	Y	N
	Number of blank rows in a frame when context B is selected (R0x0C8[1] = 1). The minimum supported value is (4 * R0x024[15] + (R0x022[2:0] + 1) * R0x022[3]). The actual vertical blanking time may be controlled by the shutter width (R0x009);				
R7:0 R0x007	13:0	0xC0	Horizontal Blanking-Context A (RW)	Y	YM
	Number of blank columns in a row when context A is selected (R0x0C8[0] = 0). The extra columns are added at the beginning of a row.				
R8:0 R0x008	14:0	0x9	Vertical Blanking-Context A (RW)	Y	N
	Number of blank rows in a frame when context A is chosen (R0x0C8[1] = 1). The minimum supported value is (4 * R0x024[15] + (R0x022[2:0]+1) * R0x022[3]). The actual vertical blanking time may be controlled by the shutter width (R0x09).				
R9:0 R0x009	15:0	0x1DC	Shutter Width (RW)	Y	N
	Integration time in number of rows. The integration time is also influenced by the shutter delay (R0x00C) and the overhead time. The user should program this register when AE/AWB/flicker are off.				

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R10:0 R0x00A	15:0	0x8011	Row Speed (RW)		
	15:14	0x2	Reserved.		
	13	0x0	Reserved.		
	8	0x0	Invert pixel clock Invert PIXCLK. When clear, FRAME_VALID and LINE_VALID are set up relative to the delayed rising edge of PIXCLK. When set, FRAME_VALID and LINE_VALID are set up relative to the delayed falling edge of PIXCLK.	N	N
	7:4	0x1	Pixel clock delay Number of half master clock cycle increments to delay the rising edge of PIXCLK relative to transitions on FRAME_VALID, LINE_VALID, and DOUT.	N	N
	3	0x0	Reserved.		
	2:0	0x1	Pixel clock speed in Mclk periods A programmed value of N gives a pixel clock period of N master clocks in full power mode and 2 * N master clocks in low power mode. A value of "0" is treated like (and reads back as) a value of "1."	Y	YM
	Relevant in Sensor Bypass Mode				
R11:0 R0x00B	15:0	0x0	Extra Delay (RW)	Y	N[1]
	Extra blanking inserted between frames. A programmed value of N increases the vertical blanking time by N pixel clock periods. Can be used to get a more exact frame rate. It may affect the integration times of parts of the image when the integration time is less than one frame. Relevant in sensor bypass mode.				
R12:0 R0x00C	15:0	0x0	Shutter Delay (RW)	Y	N
	The amount of time from the end of the sampling sequence to the beginning of the pixel reset sequence. If the value in this register exceeds the row time, the reset of the row does not complete before the associated row is sampled, and the sensor does not generate an image. A programmed value of N reduces the integration time by (N/2) pixel clock periods in low power mode and by N pixel clock periods in full power mode. User should program register when AE/AWB/flicker are off.				

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R13:0 R0x00D	15:0	0x8	Reset (RW)		
	15	0x0	Synchronize changes When this bit is returned to "0," all pending register updates are made on the next frame start. By default, the update of many of the registers is synchronized to frame start. Setting this bit inhibits this update; register changes remain pending until this bit is returned to "0."	N	N
	13	0x0	Reserved.		
	10	0x0	Swap Two-Wire Serial Interface ID 0: By default, the sensor serial bus responds to addresses 0xBA and 0xBB (for SADDR signal = 1). 1: The sensor serial bus responds to addresses 0x90 and 0x91 (for SADDR signal = 1). The addresses are opposite for SADDR signal = 0. Writes to this bit are ignored when STANDBY is asserted.	N	N
	9	0x0	Restart bad frames When set, a restart is forced to take place whenever a bad frame is detected. This can shorten the delay when waiting for a good frame since the delay, when masking out a bad frame and performing a restart, is the integration time rather than the full frame time.	N	N
	8	0x0	Show bad frames 0: Output only good frames (default). 1: Output all frames (including bad frames). A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, zoom, row or column skip, binning, mirroring, or use of border.	N	N
	7	0x0	Inhibit standby from signal By default, asserting the STANDBY signal places the sensor in a low-power state. Setting this bit stops the STANDBY signal from affecting entry to or exit from the low-power state.	N	N
	6	0x0	Drive signals By default, asserting STANDBY causes the signal interface to enter a High-Z. Setting this bit stops STANDBY from contributing to output-enable control.	N	N
	5	0x0	Reset SOC Registers	N	
	4	0x0	Output disable 0: Output signals' state is determined by R0x00D[6] and STANDBY/VDD_DIS signal states. 1: All output signals become high impedance state.		
	3	0x1	Chip Enable 0: Stop sensor readout. To put the part in low power mode, enter standby mode and disable the master clock to the sensor. 1: Normal operation. When this bit is returned to "1," sensor readout restarts and starts resetting the starting row in a new frame.	N	N
	2	0x0	Standby Setting this bit places the sensor in a low-power state.	N	YM
	1	0x0	Restart sensor Setting this bit causes the sensor to truncate the current frame and start resetting the first row. The delay before the first valid frame is read out is equal to the integration time. This bit is write-1 but always reads back as "0."	N	YM

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
	0	0x0	Reset Registers Setting this bit puts the sensor in reset; the frame being generated is truncated and the signal interface goes to an idle state. All internal registers (except for this bit) go to the default power-up state. Clearing this bit resumes normal operation.	N	YM
R31:0 R0x01F	15:0	0x0	FRAME_VALID Control (RW)		
	15	0x0	Enable early frame valid fall 0: Default. FRAME_VALID goes low six pixel clocks after last LINE_VALID. 1: Enables the early disabling of FRAME_VALID as set in R0x01F[14:8]. LINE_VALID is still generated for all active rows.	N	N
	14:8	0x0	Down rows before When enabled, the FRAME_VALID falling edge occurs within the programmed number of rows before the end of the last LINE_VALID: (1 + R0x01F[14:8]) * row time + constant (constant = 3 in default mode) The value of this field must not be larger than row width R0x003.	N	N
	7	0x0	Enable early frame valid rise 0: Default. FRAME_VALID goes high 6 pixel clocks before first LINE_VALID. 1: Enables the early rise of FRAME_VALID as set in R0x01F[6:0].	N	N
	6:0	0x0	Up rows before When enabled, the FRAME_VALID rising edge is set HIGH the programmed number of rows before the first LINE_VALID: (1 + bits 6:0)*row time + horizontal blank + constant (constant = 3 in default mode).	N	N
	Relevant in Sensor Bypass Mode.				
R32:0 R0x020	15:0	0x100	Read Mode-Context B (RW)		
	15	0x0	Binning Context B When Read mode Context B is selected (R0x0C8[3] = 1): 0: Normal operation. 1: Binning enabled.	Y	YM
	13	0x0	Reserved.		
	12:11	0x0	Reserved.		
	10	0x0	Power mode Context B When Read mode context B is selected (R0x0C8[3] = 1): 0: Read out at maximum speed. 1: Read out at half speed to reduce power. Maximum readout frequency is now half the master clock frequency, and the pixel clock is automatically adjusted as described for the pixel clock speed register.	Y	YM

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R32:0 R0x020	8	0x1	Oversized When this bit is set, a four pixel border is output around the active image array independent of readout mode (skip, zoom, mirror, etc.). Setting this bit adds eight to the number of rows and columns in the frame. This setting applies to both context A and B.	Y	YM
	7:6	0x0	Column Skip Context B When Read mode context B is selected (R0x0C8[3] = 1) and column skip is enabled (bit 7 = 1): 00: Column Skip 2x. 01: Column Skip 4x. Not supported in SOC mode. 10: Column Skip 8x. Not supported in SOC mode. 11: Column Skip 16x. Not supported in SOC mode.	Y	YM
	5:4	0x0	Row Skip Context B When Read mode context B is selected (R0x0C8[3] = 1) and Row skip is enabled (bit 4 = 1): 00: Row Skip 2x. 01: Row Skip 4x. Not supported in SOC mode. 10: Row Skip 8x. Not supported in SOC mode. 11: Row Skip 16x. Not supported in SOC mode.	Y	YM
	3	0x0	Column Skip Enable Context B When Read mode context B is selected (R0x0C8[3] = 1): 0: Normal readout. 1: Enable column skip.	Y	YM
	2	0x0	Row Skip Enable Context B When Read mode context B is selected (R0x0C8[3] = 1): 0: Normal readout. 1: Enable row skip.	Y	YM
	1	0x0	Mirror columns Read out columns from right to left (mirrored). When set, column readout starts from column (Column Start + Column Size) and continues down to (Column Start + 1). When clear, readout starts at Column Start and continues to (Column Start + Column Size - 1). This ensures that the starting color is maintained. This setting applies to both context A and B.	Y	YM
	0	0x0	Mirror rows Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Row Size) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Row Size - 1). This ensures that the starting color is maintained. This setting applies to both context A and B.	Y	YM

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R33:0 R0x021	15:0	0x8400	Read Mode-Context A (RW)		
	15	0x1	Binning Context A When Read mode context A is selected (R0x0C8[3] = 0): 0: Normal operation.	Y	YM
	10	0x1	Power mode Context A When Read mode context A is selected (R0x0C8[3] = 0): 0: Read out at maximum speed. 1: Read out at half speed to reduce power. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register.	Y	YM
	7:6	0x0	Column Skip Context A When Read mode context A is selected (R0x0C8[3] = 0) and column skip is enabled (bit 7 = 1): 00: Column Skip 2x. 01: Column Skip 4x. Not supported in SOC mode. 10: Column Skip 8x. Not supported in SOC mode. 11: Column Skip 16x. Not supported in SOC mode.	Y	YM
	5:4	0x0	Row Skip Context A When Read mode context A is selected (R0x0C8[3] = 0) and Row skip is enabled (bit 4 = 1): 00: Row Skip 2x. 01: Row Skip 4x. Not supported in SOC mode. 10: Row Skip 8x. Not supported in SOC mode. 11: Row Skip 16x. Not supported in SOC mode.	Y	YM
	3	0x0	Column Skip Enable Context A When Read mode context A is selected (R0x0C8[3] = 0): 0: Normal readout. 1: Enable column skip.	Y	YM
	2	0x0	Row Skip Enable Context A When Read mode context A is selected (R0x0C8[3] = 0): 0: Normal readout. 1: Enable row skip.	Y	YM

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R34:0 R0x022	15:0	0xD0F	Dark Columns/Rows (RW)		
	11	0x1	Number of Dark Columns in Binning Mode MT9M112 has 80 dark columns used for the row-wise noise correction algorithm. In binning mode: 0: Read out 24 dark column pairs(4–51). 1: Read out 40 dark column pairs(4–83).	N	N
	10	0x1	Number of dark columns in image MT9M112 has 80 dark columns used for the row-wise noise correction algorithm. In non-binning mode: 0: Read out 40 dark columns (4–43). 1: Read out 72 dark columns (4–75).	N	N
	9	0x0	Show dark columns in image When set, the 72/40/24 (dependent on bit 10 and binning mode) dark columns are output before the active pixels in a line. The dark columns are usually read out during horizontal blank. The horizontal blanking time is therefore decreased by the same amount that is added to the active line when this bit is enabled. Not supported in SOC mode.	N	N
	8	0x1	Read dark columns 0: When disabled, an arbitrary number of dark columns can be read out by including them in the active image. Enabling the dark columns increases the minimum value for horizontal blanking but does not affect the row time. 1: Enables the readout of dark columns for use in the row-wise noise correction algorithm. The number of columns used are determined by bits 11-10 and binning mode.	N	Y
	7	0x0	Show dark rows in image When set, the programmed dark rows is output before the active window along with the extra rows between the dark and active rows. FRAME_VALID is thus asserted earlier than normal. This has no effect on integration time or frame rate. Not supported in SOC mode.	N	N
	6:4	0x0	Dark row start address The start address for the dark rows within the eight available rows. Must be set so all dark rows read out falls in the address space 7:0.	N	N
	3	0x1	Reserved.		
	2:0	0x7	Number of dark rows A value of N causes (n+1) dark rows to be read out at the start of each frame when dark row readout is enabled (bit 3).	N	Y

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R35:0 R0x023	15:0	0x0E08	Flash Control (RW)		
	15	RO	Flash SHUTTER signal Reflects the current state of the FLASH output signal.		
	14	RO	Flash Triggered Indicates that the FLASH output signal is asserted for the current frame.		
	13	0x0	Enable Xenon flash Enable Xenon flash. When set, the FLASH output signal asserts for the programmed period (bits 7:0) during vertical blank. This is achieved by keeping the integration time equal to one frame and the pulse width less than the vertical blank time.	Y	N
	12:11	0x1	Flash Frame Delay Delay of the flash pulse measured in frames.	N	N
	10	0x1	Xenon Flash After Reset 0: In Xenon mode the flash is triggered after the readout of a frame. 1: In Xenon mode the flash is triggered after the resetting of a frame.	N	N
	9	0x1	Fire Flash Every Frame 0: Flash should be enabled for one frame only. 1: Flash should be enabled every frame.	N	N
	8	0x0	Enable LED flash When set, the FLASH output signal asserts prior to the start of the resetting of a frame and remains asserted until the end of the readout of the frame.	Y	Y
	7:0	0x8	Xenon Count Length of FLASH pulse when Xenon flash is enabled. The value specifies the length in units of 1024 * PIXCLK cycle increments. When the Xenon count is set to its maximum value (0xFF), the FLASH pulse is automatically truncated prior to the readout of the first row, giving the longest pulse possible.	N	N
	This is a flash control register. During normal operating mode (SOC mode), only the Xenon count control R0x023[7:0] is valid. The remaining bits R0x023[15:8] are reserved: write back the same value read for the reserve bits.				
R36:0 R0x024	15:0	0x8000	Extra Reset (RW)		
	15	0x1	Extra 2+2 row operations for anti-blooming 0: Only programmed window (set by R0x001 through R0x004) and black pixels are read. 1: Two additional rows are read and reset above and below programmed window to prevent blooming to active area.	N	N
	14	0x0	Next row reset When set, and the integration time is less than one frame time, row (n+1) is reset immediately prior to resetting row (n). This is intended to prevent blooming across rows under conditions of very high illumination.	N	N
	13:0	0x0	Reserved.		

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R37:0 R0x025	15:0	0x0	LINE_VALID Control (RW)		
	15	0x0	XOR line valid 0: Normal LINE_VALID (default, no XORing of LINE_VALID). Ineffective if continuous LINE_VALID is set. 1: LINE_VALID = "continuous" LINE_VALID XOR FRAME_VALID.	N	N
	14	0x0	Continuous line valid 0: Normal LINE_VALID (default, no LINE_VALID during vertical blank). 1: "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blank).	N	N
	Relevant in Sensor Bypass Mode.				
R43:0 R0x02B	14:0	0x20	Green1 Gain (RW)		
	14:12	0x0	Digital gain Total gain = (R0x02B[14] + 1) * (R0x02B[13] + 1) * (R0x02B[12] + 1) * Analog gain (each bit gives 2x gain).	Y	N
	11:9	0x0	Reserved.		
	8:0	0x20	Analog Gain Initial gain = R0x02B[6:0] * 0.03125 Analog gain = (R0x02B[8] + 1) * (R0x02B[7] + 1) * Initial gain	Y	N
	User should program register when AE/AWB/flicker are off.				
R44:0 R0x02C	14:0	0x20	Blue Gain (RW)		
	14:12	0x0	Digital gain Total gain = (R0x02C[14] + 1) * (R0x02C[13] + 1) * (R0x02C[12] + 1) * Analog gain (each bit gives 2x gain).	Y	N
	11:9	0x0	Reserved.		
	8:0	0x20	Analog Gain Initial gain = R0x02C[6:0] * 0.03125 Analog gain = (R0x02C[8] + 1) * (R0x02C[7] + 1) * Initial gain	Y	N
	User should program register when AE/AWB/flicker are off.				
R45:0 R0x02D	14:0	0x20	Red Gain (RW)		
	14:12	0x0	Digital Gain Total gain = (R0x02D[14] + 1) * (R0x02D[13] + 1) * (R0x02D[12] + 1) * Analog gain (each bit gives 2x gain).	Y	N
	11:9	0x0	Reserved.		
	8:0	0x20	Analog Gain Initial gain = R0x02D[6:0] * 0.03125 Analog gain = (R0x02D[8] + 1) * (R0x02D[7] + 1) * Initial gain	Y	N
	User should program register when AE/AWB/flicker are off.				
R46:0 R0x02E	14:0	0x20	Green2 Gain (RW)		
	14:12	0x0	Digital gain Total gain = (R0x02E[14] + 1) * (R0x02E[13] + 1) * (R0x02E[12] + 1) * Analog gain (each bit gives 2x gain).	Y	N
	11:9	0x0	Reserved.		
	8:0	0x20	Analog Gain Initial gain = R0x02E[6:0] * 0.03125 Analog gain = (R0x02E[8] + 1) * (R0x02E[7] + 1) * Initial gain	Y	N
	User should program this register when AE/AWB/flicker are off.				

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R47:0 R0x02F	15:0	0x20	Global Gain (RW)		
	15	0x0	Reserved.		
	14:12	0x0	Digital gain Total gain = (R0x02F[12] + 1) * (BR0x02F[13] + 1) * (R0x02F[14] + 1) * Analog Gain (each bit gives 2x gain).	Y	N
	11:9	0x0	Reserved.		
	8:0	0x20	Analog Gain This register can be used to simultaneously set all four gains. When read, it returns the value stored in R0x02B.	Y	N
	This register can be used to set all four gains at once. When read, it will return the value stored in R0x02B.				
R48:0 R0x030	14:0	0x42A	Row Noise (RW)		
	14:12	0x0	Gain threshold When the upper analog gain bits are equal to or larger than this threshold, the dark column average is used in the row noise correction algorithm. Otherwise, the subtracted value is determined by R0x030[11]. Each color is independently compared; the row noise correction algorithm is turned off for the lower gains without affecting the black level.	N	N
	11	0x0	Use black level average 0: Use mean of black level programmed threshold in the row noise correction algorithm for low gains. 1: Use black level frame average from the dark rows in the row noise correction algorithm for low gains. Note: this frame average was taken before the last adjustment of the offset DAC for that frame, so it might be slightly off.	N	Y
	10	0x1	Enable Correction 0: Normal operation. 1: Enable row noise cancellation algorithm. When this bit is set, the average value of the dark columns read out is used as a correction for the whole row. The dark average is subtracted from each pixel on the row, and then a constant is added (R0x030[9:0]).	N	Y
	9:0	0x2A	Row noise constant Constant used in the row noise cancellation algorithm. It should be set to the dark level targeted by the black level algorithm plus the noise expected between the averaged values of the dark columns. The default constant is set to 42 LSB.	N	Y
R89:0 R0x059	7:0	0xFF	Black rows (RW)	N	N
	For each bit set, the corresponding dark row (rows 4–11) are used in the black level algorithm. For this to occur, the reading of those rows must be enabled by the settings in R0x022.				
R91:0 R0x05B	6:0	RO	Dark Green1 Average (RO)		
	The frame-averaged green1 black level that is used in the black level calibration algorithm.				
R92:0 R0x05C	6:0	RO	Dark Blue Average (RO)		
	The frame-averaged blue black level that is used in the black level calibration algorithm.				
R93:0 R0x05D	6:0	RO	Dark Red Average (RO)		
	The frame-averaged red black level that is used in the black level calibration algorithm.				
R94:0 R0x05E	6:0	RO	Dark Green2 Average (RO)		
	The frame-averaged green2 black level that is used in the black level calibration algorithm.				

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R95:0 R0x05F	14:0	0x231D	Calibration Threshold (RW)		
	14:8	0x23	Thres_hi Upper threshold for targeted black level in ADC LSBs.	N	N
	6:0	0x1D	Thres_lo Lower threshold for targeted black level in ADC LSBs.	N	N
R96:0 R0x060	15:0	0x80	Calibration Control (RW)		
	15	0x0	Disable rapid sweep mode Disables the rapid sweep mode in the black level algorithm. The averaging mode remains enabled.	Y	N
	12	0x0	Recalculate When set, the rapid sweep mode is triggered if enabled, and the running frame average is reset to the current frame average. This bit is write-1, but always reads back as "0."	Y	N
	10	0x0	Reserved.		
	9	0x0	Reserved.		
	8	0x0	Enable calibration sweep mode 1: the calibration value is increased by one every frame, and all channels are the same. This can be used to get a ramp input to the ADC from the calibration DACs.	N	N
	7:5	0x4	Frames to average over Two to the power of this value determines how many frames to average when the black level algorithm is in the averaging mode. In this mode, the running frame average is calculated from the following formula: Running frame average = old running frame average - (old running frame average) / 2n + (new frame average) / 2n.	N	N
	4	0x0	Keep step size at 1 0: start at a higher step size when in rapid sweep mode, to converge faster to the correct value. 1: Step size is forced to "1" for the rapid sweep algorithm.	N	N
	3	0x0	Reserved.		
	2	0x0	Use red calibration value for blue When this bit is set, the same calibration value is used for red and blue pixels: Calibration blue = calibration red.	N	Y
	1	0x0	Use green1 calibration value for green2 When this bit is set, the same calibration value is used for all green pixels: Calibration green2 = calibration green1.	N	Y
	0	0x0	Manual Override auto black level Manual override of black level correction. 0: Normal operation (default). 1: Override automatic black level correction with programmed values. (R0x061–R0x064).	N	Y

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R97:0 R0x061	8:0	0x0	Calibration Green1 (RW)	N	Y
	Analog calibration offset for green1 pixels, represented as a two's complement signed 8-bit value. If R0x061[8] = 0, the offset is positive and the magnitude is given by R0x061[7:0]. If R0x061[8] = 1, the offset is negative and the magnitude is given by not (R0x061[7:0]) + 1). If R0x060[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x060[0] = 1, this register is R/W and can be used to set the calibration offset manually. Green1 pixels share rows with red pixels.				
R98:0 R0x062	8:0	0x0	Calibration Blue (RW)	N	Y
	Analog calibration offset for blue pixels, represented as a two's complement signed 8-bit value. If R0x062[8] = 0 the offset is positive and the magnitude is given by R0x062[7:0]. If R0x062[8] = 1, the offset is negative and the magnitude is given by not (R0x062[7:0]) + 1). If R0x060[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x060[0] = 1, this register is R/W and can be used to set the calibration offset manually.				
R99:0 R0x063	8:0	0x0	Calibration Red (RW)	N	Y
	Analog calibration offset for red pixels, represented as a two's complement signed 8-bit value. If R0x063[8] = 0, the offset is positive and the magnitude is given by R0x063[7:0]. If R0x063[8] = 1, the offset is negative and the magnitude is given by not (R0x063[7:0]) + 1). If R0x060[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x060[0] = 1, this register is R/W and can be used to manually set the calibration offset.				
R100:0 R0x064	8:0	0x0	Calibration Green2 (RW)	N	Y
	Analog calibration offset for green2 pixels, represented as a two's complement signed 8-bit value. if R0x064[8] = 0, the offset is positive and the magnitude is given by R0x064[7:0]. If R0x064[8] = 1, the offset is negative and the magnitude is given by not (R0x064[7:0]) + 1.) If R0x060[0] = 0, this register is RO and returns the current value computed by the black level calibration algorithm. If R0x060[0] = 1, this register is R/W and can be used to manually set the calibration offset. Green2 pixels share rows with blue pixels.				

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R101:0 R0x065	15:0	0xE000	Clock Control (RW)		
	15	0x1	PLL bypass 0: Use clock produced by PLL as master clock. 1: Bypass the PLL. Use CLKIN port as master clock.	N	N
	14	0x1	PLL power down 0: PLL powered-up. 1: Keep PLL in power-down to save power (default).	N	N
	13	0x1	Power down PLL during standby (bit14 = 0) This register only has an effect when bit 14 = 0. 0: PLL powered-up during Standby. 1: Turn off PLL (power-down) during Standby to save power (default).	N	N
	12	0x0	Soft PLL Reset 0: PLL not in reset state. 1: Set PLL in reset state.	N	N
	11	0x0	Reserved.		
	3	0x0	Reserved.		
	2	0x0	Reserved.		
	1	0x0	Reserved.		
	0	0x0	Reserved.		
R102:0 R0x066	15:0	0x1E01	PLL control 1 (RW)		
	15:8	0x1E	M Parameter of PLL M value for PLL must be 16 or higher.	N	N
	5:0	0x1	N Parameter of PLL N Value for PLL	N	N
	PLL control 1				
R103:0 R0x067	11:0	0x501	PLL control 2 (RW)		
	11:8	0x5	Reserved.		
	6:0	0x1	P Parameter of PLL P value for PLL.	N	N
	PLL control 2				
R104:0 R0x068	6:0	0x5D	IO Slew Rate Control (RW)		
	6:4	0x5	Slew rate control for PIXCLK signal. Eight slew rates (code 0–code 7) are selectable. Code 0 is the slowest; code 7 is the fastest. Rise time and fall time are matched. Refer to the Electrical section for more details.	N	N
	3	0x1	Input PAD Power down input stage of output only pads.	N	N
	2:0	0x5	Slew rate control for DOUT0–DOUT7, DOUTLSB0–DOUTLSB1, FRAME_VALID, LINE_VALID, SDATA, FLASH, and SHUTTER signals. Eight slew rates (code 0–code 7) are selectable. Code 0 is the slowest; code 7 is the fastest. Rise time and fall time are matched. Refer to the "Electrical Specifications" on page 103 for more details.	N	N

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R192:0 R0x0C0	15:0	0x0	Global Shutter Control (RW)		
	15	0x0	GRST enable Enter global reset. This bit is write-1 only and is always read 0.	N	N[2]
	2	0x0	FLASH control 0: FLASH is deasserted by R0x0B6 (deassert FLASH). 1: FLASH is deasserted at end of readout.	N	N
	1	0x0	SHUTTER signal control 0: SHUTTER signal is deasserted by R0x0C4 (deassert shutter). 1: SHUTTER signal is deasserted at end of readout.	N	N
	0	0x0	Readout control 0: Start of readout is controlled by R0x0C2 (start readout time). 1: Start of readout is controlled by falling edge of GRST_CTR signal.	N	N
R193:0 R0x0C1	15:0	0x4B	Start Integration (T1) (RW)	N	N
	These 16 bits are compared to the upper bits of a 24-bit counter, which starts counting master clocks when global reset starts. When this value is reached, global reset is deasserted, and integration time starts. Note: there is a minimum time period for which global reset is always held. This time is defined by the physical properties of the boost circuit. The minimum time the digital logic waits is actually programmable in R0x0C7.				
R194:0 R0x0C2	15:0	0x4B	Start Readout (T2) (RW)	N	N
	These 16 bits are added to R0x0C1 (start integration time) and compared to the 24-bit counter mentioned for R0x0C1. The value defines the time from when integration time starts to when it is guaranteed to end. Readout then commences.				
R195:0 R0x0C3	15:0	0x71	Assert SHUTTER signal (T3) (RW)	N	N
	These 16 bits are compared to the upper bits of a 24-bit counter, which starts counting master clocks when global reset starts. When this value is reached, the SHUTTER signal is asserted.				
R196:0 R0x0C4	15:0	0x96	Deassert SHUTTER signal (T4) (RW)	N	N
	These 16 bits are compared to the upper bits of a 24-bit counter, which starts counting master clocks when global reset starts. When this value is reached, the SHUTTER signal is deasserted if SHUTTER signal control is 0 (R0x0C0[1]).				
R197:0 R0x0C5	15:0	0x4B	Assert flash (RW)	N	N
	These 16 bits are compared to the upper bits of a 24-bit counter, which starts counting master clocks when global reset starts. When this value is reached, the flash is asserted.				
R198:0 R0x0C6	15:0	0x5A	Deassert Flash (RW)	N	N
	These 16 bits are compared to the upper bits of a 24-bit counter, which starts counting master clocks when global reset starts. When this value is reached, the flash is deasserted if flash control is 0 (R0x0C0[2]).				

Table 15: Page 0: Sensor Core Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description	Sync'd to Frame Start	Bad Frame
R200:0 R0x0C8	15:0	0x0	Context Control (RW)		
	15	0x0	Restart Setting this bit causes the sensor to abandon the current frame and start resetting the first row. Same physical register as R0x00D[1].	N	YM
	7	0x0	Enable Xenon flash Enable Xenon flash. Same physical register as R0x023[13].	Y	N
	3	0x0	Read mode select 0: Use Read mode context A, R0x021. 1: Use Read mode context B, R0x020. Bits only found in Read mode context B register are always taken from that register.	Y	YM
	2	0x0	Enable LED flash Enable LED flash. Same physical register as R0x023[8].	Y	Y
	1	0x0	Vertical blank select 0: Use Vertical Blank context A, R0x008. 1: Use Vertical Blank context B, R0x006.	Y	YM
	0	0x0	Horizontal blank select 0: Use Horizontal Blank context A, R0x007. 1: Use Horizontal Blank context B, R0x005.	Y	YM
R240:0 R0x0F0	2:0	0x0	Page Map (RW)		
	2:0	0x0	Page Address: 000: Sensor address page. 001: Colorpipe Address page. 010: Camera control address page. 011–111: Reserved.	N	N
	This register specifies the memory address page for the two-wire interface protocol.				
R241:0 R0x0F1	15:0	0x0	Byte Wise Address (RW)	N	N
	Use this register to perform reads and writes to the sensor in two 8-bit serial transmissions instead of one 16-bit.				
R255:0 R0x0FF	15:0	0x148C	Chip Version (RO)		
	Chip version.				

Notes: 1. R0x00B: Unless integration time is less than one frame.
2. R0x0C0[15]: Will cause current frame to stop if triggered during a frame.

Page 1: Image Processing Register Descriptions

Table 16: Page 1: Image Processing Register Descriptions
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R0:1 R0x100	3:0	X	Module ID (RO)
	This register returns the GPI[3:0] signal state. It is typically used for module ID by the module manufacturer.		
R5:1 R0x105	3:0	0xB	Aperture Correction [sharpening] Gain (RW)
	3	0x1	Enable Auto Sharpening Refer to R0x233 to set thresholds.
	2:0	0x3	Sharpening Gain Sharpening factor: 000: No sharpening. 001: 25% sharpening. 010: 50% sharpening. 011: 75% sharpening. 100: 100% sharpening. 101: 125% sharpening. 110: 150% sharpening. 111: 200% sharpening.
	Aperture correction scale factor used for sharpening.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R6:1 R0x106	15:0	0x600E	Mode Control (RW)
	15	0x0	Manual White Balance 0: Disables manual white balance. 1: Enables manual white balance. User can set the base matrix and color channel gains. This bit must be asserted and deasserted with a frame in between or use R0x228[12] to force new color-correction settings to take effect.
	14	0x1	Auto Exposure 0: Disables auto exposure. 1: Enables auto exposure.
	13	0x1	Defect Correction 0: Disables on-the-fly defect correction. 1: Enables on-the-fly defect correction.
	12	0x0	Clip Aperture Correction 0: Do not clip aperture correction. 1: Clip aperture correction. Small aperture corrections (< 32) are attenuated to reduce noise amplification.
	11	0x0	Reserved.
	10	0x0	Lens Shading Correction 0: Disables lens-shading correction. 1: Enables lens-shading correction.
	9	0x0	Reserved.
	8	0x0	Reserved.
	7	0x0	Auto Flicker Detection Enables flicker detection. 0: Disables automatic flicker detection. 1: Enables automatic flicker detection.
	5	0x0	Reserved.
	4	0x0	Bypass Color Processing Bypasses the color correction matrix. 0: Normal color processing. 1: Outputs "raw" color bypassing color correction matrix.
	3:2	0x3	Auto Exposure Window Ctrl - Backlight compensation Auto exposure backlight compensation control. 00: Auto exposure sampling window is specified by R0x226 and R0x227 ("full window"). 01: Auto exposure sampling window is specified by R0x22B and R0x22C ("center window"). 1x: Auto exposure sampling window is specified by the weighted sum of the full window and the center window, with the center window weighted four times more heavily.
	1	0x1	AWB Control Enables auto white balance. 0: Stops auto white balance updates. 1: Enables auto white balance.
	0	0x0	Reserved.
	This register specifies the operating mode of the IFP.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R8:1 R0x108	10:0	0x80	Format Control (RW)
	10	0x0	Clock Disable / Enable During Blanking 0: Clock enabled during blanking. 1: Clock disabled during blanking.
	9	0x0	Flip Bayer Column Flip Bayer columns in processed Bayer output mode. 0: Column order is green, red (first rows) and blue, green (second rows). 1: Column order is red, green and green, blue.
	8	0x0	Flip Bayer Row Flip Bayer rows in processed Bayer output mode. 0: First row contains green and red; the second row contains blue and green. 1: First row contains blue and green; the second row contains green and red.
	7	0x1	ITU-R BT.656 Protection Bits Controls the values used for the protection bits in Rec. ITU-R BT.656 codes. 0: Use zeros for the protection bits. 1: Use the correct values.
	5	0x0	Monochrome Test Mode Enable In YCbCr mode, the Chroma values are cleared to zero: Cb=Cr=0. In RGB mode, red and blue values are set equal to the green value.
	4	0x0	Disable Cb or Blue Disables Cb color output channel (Cb = 128) in YCbCr mode and disables the blue color output channel (B = 0) in RGB mode. 0: Normal Cb or B output. 1: Forces Cb to 128 or B to 0.
	3	0x0	Disable Y or Green Disables Y color output channel (Y = 128) in YCbCr and disables the green color output channel (G = 0) in RGB mode. 0: Normal Y or G output. 1: Forces Y to 128 or G to 0.
	2	0x0	Disable Cr or Red Disables Cr color output channel (Cr = 128) in YCbCr mode and disables the red color output channel (R = 0) in RGB mode. 0: Normal Cr or R output. 1: Forces Cr to 128 or R to 0.
	1	0x0	Bayer CFA [Vertical Shift] Toggles the assumptions about Bayer vertical CFA shift. 0: Row containing red comes first. 1: Row containing blue comes first.
	0	0x0	Bayer CFA [Horizontal Shift] Toggles the assumptions about Bayer horizontal CFA shift. 0: Column containing Blue comes first. 1: Column containing Red comes first.
	This register specifies the output timing and format in conjunction with R0x13A or R0x19B (depending on the context).		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R37:1 R0x125	6:0	0x4D	Saturation Adjustment (RW)
	6:3	0x9	Overall Attenuation of Saturation Specifies overall attenuation of color saturation. 0000: Full color saturation. 0001: 75% of full saturation. 0010: 50% of full saturation. 0011: 37.5% of full saturation. 0100: 25% of full saturation. 1001: 112.5% of full saturation. 1010: 125% of full saturation. 1011: 137.5% of full saturation. 0101: 150% of full saturation. 0110: Black and white.
	2:0	0x5	Attenuation at High Luminance Specifies color saturation attenuation at high luminance (linearly increasing attenuation from no attenuation to monochrome at luminance of 224). 000: No attenuation. 001: Attenuation starts at luminance of 216. 010: Attenuation starts at luminance of 208. 011: Attenuation starts at luminance of 192. 100: Attenuation starts at luminance of 160. 101: Attenuation starts at luminance of 96.
	This register specifies the color saturation control settings.		
R52:1 R0x134	15:0	0x0	Luma Offset [Brightness Control] (RW)
	15:8	0x0	RGB Offset in RGB Mode Offset applied to RGB channels in RGB mode.
	7:0	0x0	Y Offset in YCbCr Mode Offset applied to Y in YCbCr mode.
	Offset applied to Luma and RGB channels prior to output.		
R53:1 R0x135	15:0	0xFF00	Clipping Limits for Output Luminance (RW)
	15:8	0xFF	Upper Limit Highest value of output luminance.
	7:0	0x0	Lower Limit Lowest value of output luminance.
	Clipping limits for output luminance.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R58:1 R0x13A	14:0	0x200	Output Format Control [Context A] (RW)
	14	0x0	Output Processed Bayer Output processed Bayer data when in RGB mode (R0x13A[8] = 1]).
	13	0x0	Reserved.
	12	0x0	SOC as Sensor. Sensor output coupled directly to SOC camera port, including two extra LSB signals to provide access to the full 10-bit sensor output. Bits [9:2] of the sensor output are mapped to DOUT[7:0]. Bits [1:0] of the sensor output are mapped to DOUT_LSB[1] and DOUT_LSB[0] respectively.
	11	0x0	ITU-R BT.656 Codes Enables embedding Rec. ITU-R BT.656 synchronization codes in the output data.
	10	0x0	Bypass IFP Entire image processing is bypassed and raw Bayer is output directly. 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface and the 10 bits are formatted to two output bytes through the camera interface; i.e., 8 + 2. Data rate is effectively the same as the default 16-bits per pixel modes. AE, AWB, and other image processing features still function and control the sensor, though they are assuming some gain or correction is performed as it passes through the colorpipe.
	9	0x1	Invert Output Pixel Clock Inverts output pixel clock. By default, this bit is set and data is sampled at the falling edge of PIXCLK for capture by the receiver on the rising edge.
	8	0x0	Output Mode Selects between RGB and YCbCr output formats. 0: Output YCbCr data. 1: Output RGB data. The format is defined by R0x13A[7:6].
	7:6	0x0	RGB Output Format 00: 16-bit RGB565. 01: 15-bit RGB555. 10: 12-bit RGB444x. 11: 12-bit RGBx444.
	5:4	0x0	Test Ramp Output 00: Off. 01: By column. 10: By row. 11: By frame.
	3	0x0	Output RGB or YCbCr Shifted up 3 Bits Output RGB or YCbCr values are shifted 3 bits up. Use with R0x13A[5:4] to test LCDs with low color depth.
	2	0x0	Average Two Nearby Chrominance Bytes
	1	0x0	Swap Output Bytes In YCbCr mode, swaps chroma and Y bytes. In RGB mode, swaps odd and even bytes.
	0	0x0	Swap Red and Blue In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels.
	Output Format Control for Context A. Refer to R0x19B for the corresponding control for Context B.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R59:1 R0x13B	10:0	0x42A	IFP Black-Level Subtraction pre Lens (RW)
	10	0x1	Enables Black-Level Subtraction Enables subtraction of black-level offset from the signal before lens-shading correction. 0: No Black-level subtraction performed. 1: Subtraction enabled.
	9:0	0x2A	Value of Black Black-level offset. Set this value to Row Noise Constant, R0x30[9:0], the black level in the signal from the sensor core. The first block of the IFP subtracts black-level offset from the sensor core signal. The objective is to remove any pedestal before lens-shading correction and auto exposure digital gains.
	Defines and enables black-level subtraction. Controls reduction of the black level pedestal in the signal from the sensor core before lens-shading correction auto exposure digital gains.		
R60:1 R0x13C	10:0	0x400	IFP Black-Level Addition post Lens (RW)
	10	0x1	Enable Black-Level Addition Enables addition of black-level offset to the lens shading corrected signal. 0: No addition performed. 1: Addition enabled.
	9:0	0x0	Value of black Black-level offset. This value is added to each pixel value, after lens-shading correction and auto exposure digital gains. Black-level addition can raise the black-level pedestal for subsequent IFP.
	Defines and enables black-level addition. Controls raising the black-level pedestal in the signal after lens-shading correction and auto exposure digital gains.		
R71:1 R0x147	15:0	0x1030	Edge Threshold for Noise Reduction (RW)
	15:8	0x10	Threshold for Green Balance or Green Noise.
	7:0	0x30	Threshold for Main Noise Reduction.
	Green Noise Reduction hides Green Imbalance making Green Balance Compensation unnecessary. This allows the same register field to be used for both Green thresholds. The Main Noise threshold affects Red, Blue and Green if the Exclude Green bit R0x19D[10] is cleared. Each algorithm can be disabled by setting its threshold to "0."		
R72:1 R0x148	7:0	0x0	Test Pattern Generator (RW)
	7	0x0	Force WB Digital Gains to Unity 0: Normal operation. 1: Force digital gains to 1.0.
	2:0	0x0	Test Pattern Selection 000: Normal operation (test pattern bypassed). 001: Vertical monochrome gradient. 111: Colorbars test pattern All other values: Flat fields of different luminances.
	This register enables test-pattern generation at the input of the image processor.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R83:1 R0x153	15:0	0xE04	Gamma Table A Knee Points Y1 Y2 (RW)
	15:8	0xE	Y2 Knee point value Y2.
	7:0	0x4	Y1 Knee point value Y1.
	This register specifies output values Y1 and Y2 for the piece-wise linear gamma correction for context A. Piece-wise linear gamma correction transforms 10-bit RGB from color processing to nonlinear 8-bit RGB for output from the chip. Pre-gamma image processing generates 10-bit RGB values ranging from 0 to 1023. Piece-wise linear gamma correction has 11 intervals with knee points corresponding to the following input values: X_i = 0... 11 = {0, 16, 32, 64, 128, 256, 384, 512, 640, 768, 896, 1024}. For each input value X_i, the user can program the corresponding output value Y_i. The valid range for Y_i is from 0 to 255. A further offset is added to the gamma-corrected values as specified in R0x134. Default values for gamma table knee points implement a gamma of 0.6.		
R84:1 R0x154	15:0	0x4C28	Gamma Table A Knee Points Y3 Y4 (RW)
	15:8	0x4C	Y4 Knee point value Y4.
	7:0	0x28	Y3 Knee point value Y3.
	This register specifies output values Y3 and Y4 for the piece-wise linear gamma correction for context A. Refer to R0x153 for a description of the gamma correction table.		
R85:1 R0x155	15:0	0x9777	Gamma Table A Knee Points Y5 Y6 (RW)
	15:8	0x97	Y6 Knee point value Y6.
	7:0	0x77	Y5 Knee point value Y5.
	This register specifies output values Y5 and Y6 for the piece-wise linear gamma correction for context A. Refer to R0x153 for a description of the gamma correction table.		
R86:1 R0x156	15:0	0xC7B1	Gamma Table A Knee Points Y7 Y8 (RW)
	15:8	0xC7	Y8 Knee point value Y8.
	7:0	0xB1	Y7 Knee point value Y7.
	This register specifies output values Y7 and Y8 for the piece-wise linear gamma correction for context A. Refer to R0x153 for a description of the gamma correction table.		
R87:1 R0x157	15:0	0xEEDB	Gamma Table A Knee Points Y9 Y10 (RW)
	15:8	0xEE	Y10 Knee point value Y10.
	7:0	0xDB	Y9 Knee point value Y9.
	This register specifies output values Y9 and Y10 for the piece-wise linear gamma correction for context A. Refer to R0x153 for a description of the gamma correction table.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R88:1 R0x158	15:0	0xFF00	Gamma Table A Knee Points Y0 Y11 (RW)
	15:8	0xFF	Y11 Knee point value Y11.
	7:0	0x0	Y0 Knee point value Y0.
	This register specifies output values Y0 and Y11 for the piece-wise linear gamma correction for context A. Refer to R0x153. for a description of the gamma correction table.		
R128:1 R0x180	4:0	X	Lens Correction Control (RW)
	4:2	X	kp/Kxy Coefficient. The coefficient, “kp” or “Kxy,” of the cross-term. A three-bit code determines the value of kp: 000: 0 001: 1 010: 2 011: 4 100–111: 8
	1:0	X	kd/Kx Scale Factor. The scaling factor, “kd” or “Kx,” for derivative, or knee, values. A two-bit code determines the value of kd: 00: 1 01: 0.5 10: 0.25 11: 0.125
R129:1 R0x181	15:0	X	Lens Vertical Red Knee 0 and Initial Value (RW)
	15:8	X	Red Vertical Derivative Value at Vertex (knee) 0.
	7:0	X	Initial Value of Red Vertical Function.
R130:1 R0x182	15:0	X	Lens Vertical Red Knees 2 and 1 (RW)
	15:8	X	Red Vertical Derivative Value at Vertex 2.
	7:0	X	Red Vertical Derivative Value at Vertex 1.
R131:1 R0x183	15:0	X	Lens Vertical Red Knees 4 and 3 (RW)
	15:8	X	Red Vertical Derivative Value at Vertex 4.
	7:0	X	Red Vertical Derivative Value at Vertex 3.
R132:1 R0x184	15:0	X	Lens Vertical Green Knee 0 and Initial Value (RW)
	15:8	X	Green Vertical Derivative Value at Vertex 0.
	7:0	X	Initial Value of Green Vertical Function.
R133:1 R0x185	15:0	X	Lens Vertical Green Knees 2 and 1 (RW)
	15:8	X	Green Vertical Derivative Value at Vertex 2.
	7:0	X	Green Vertical Derivative Value at Vertex 1.
R134:1 R0x186	15:0	X	Lens Vertical Green Knees 4 and 3 (RW)
	15:8	X	Green Vertical Derivative Value at Vertex 4.
	7:0	X	Green Vertical Derivative Value at Vertex 3.
R135:1 R0x187	15:0	X	Lens Vertical Blue Knee 0 and Initial Value (RW)
	15:8	X	Blue Vertical Derivative Value at Vertex 0.
	7:0	X	Initial Value of Blue Vertical Function.

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R136:1 R0x188	15:0	X	Lens Vertical Blue Knees 2 and 1 (RW)
	15:8	X	Blue Vertical Derivative Value at Vertex 2.
	7:0	X	Blue Vertical Derivative Value at Vertex 1.
R137:1 R0x189	15:0	X	Lens Vertical Blue Knees 4 and 3 (RW)
	15:8	X	Blue Vertical Derivative Value at Vertex 4.
	7:0	X	Blue Vertical Derivative Value at Vertex 3.
R138:1 R0x18A	15:0	X	Lens Horizontal Red Knee 0 and Initial Value (RW)
	15:8	X	Red Horizontal Derivative Value at Vertex 0.
	7:0	X	Initial Value of Red Horizontal Function.
R139:1 R0x18B	15:0	X	Lens Horizontal Red Knees 2 and 1 (RW)
	15:8	X	Red Horizontal Derivative Value at Vertex 2.
	7:0	X	Red Horizontal Derivative Value at Vertex 1.
R140:1 R0x18C	15:0	X	Lens Horizontal Red Knees 4 and 3 (RW)
	15:8	X	Red Horizontal Derivative Value at Vertex 4.
	7:0	X	Red Horizontal Derivative Value at Vertex 3.
R141:1 R0x18D	7:0	X	Lens Horizontal Red Knee 5 (RW)
	7:0	X	Red Horizontal Derivative Value at Vertex 5.
R142:1 R0x18E	15:0	X	Lens Horizontal Green Knee 0 and Initial Value (RW)
	15:8	X	Green Horizontal Derivative Value at Vertex 0.
	7:0	X	Initial Value of Green Horizontal Function.
R143:1 R0x18F	15:0	X	Lens Horizontal Green Knees 2 and 1 (RW)
	15:8	X	Green Horizontal Derivative Value at Vertex 2.
	7:0	X	Green Horizontal Derivative Value at Vertex1.
R144:1 R0x190	15:0	X	Lens Horizontal Green Knees 4 and 3 (RW)
	15:8	X	Green Horizontal Derivative Value at Vertex 4.
	7:0	X	Green Horizontal Derivative Value at Vertex 3.
R145:1 R0x191	7:0	X	Lens Horizontal Green Knee 5 (RW)
	7:0	X	Green Horizontal Derivative Value at Vertex 5.
146:1 R0x192	15:0	X	Lens Horizontal Blue Knee 0 and Initial Value (RW)
	15:8	X	Blue Horizontal Derivative Value at Vertex 0.
	7:0	X	Initial Value of Blue Horizontal Function.
R147:1 R0x193	15:0	X	Lens Horizontal Blue Knees 2 and 1 (RW)
	15:8	X	Blue Horizontal Derivative Value at Vertex 2.
	7:0	X	Blue Horizontal Derivative Value at Vertex 1.
R148:1 R0x194	15:0	X	Lens Horizontal Blue Knees 4 and 3 (RW)
	15:8	X	Blue Horizontal Derivative Value at Vertex 4.
	7:0	X	Blue Horizontal Derivative Value at Vertex 3.
R149:1 R0x195	7:0	X	Lens Horizontal Blue Knee 5 (RW)
	7:0	X	Blue Horizontal Derivative Value at Vertex 5.
R153:1 R0x199	15:0	RO	Line Counter (RO)
	Use line counter to determine the number of the line currently being output.		
R154:1 R0x19A	15:0	RO	Frame Counter (RO)
	Use frame counter to determine the index of the frame currently being output.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R155:1 R0x19B	15:0	0x200	Output Format Control [Context B] (RW)
	14	0x0	Output Processed Bayer Output processed Bayer data when in RGB mode (R0x19B[8] = 1]).
	13	0x0	Reserved.
	12	0x0	SOC as Sensor
	11	0x0	ITU-R BT.656 Codes Enables embedding Rec. ITU-R BT.656 synchronization codes in the output data.
	10	0x0	Bypass IFP Entire image processing is bypassed and raw Bayer is output directly. 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface and the 10 bits are formatted to two output bytes through the camera interface; i.e., 8 + 2. Data rate is effectively the same as the default 16-bits per pixel modes. AE, AWB, and other image processing features still function and control the sensor, though they are assuming some gain or correction is performed as it passes through the colorpipe.
	9	0x1	Invert Output Pixel Clock Inverts output pixel clock. By default, this bit is set and data is sampled at the falling edge of PIXCLK for capture by the receiver on the rising edge.
	8	0x0	Output Mode Selects between RGB and YCbCr output formats. 0: Output YCbCr data. 1: Output RGB data. The format is defined by R0x19B[7:6].
	7:6	0x0	RGB Output Format 00: 16-bit RGB565. 01: 15-bit RGB555. 10: 12-bit RGB444x. 11: 12-bit RGBx444.
	5:4	0x0	Test Ramp Output 00: Off. 01: By column. 10: By row. 11: By frame.
	3	0x0	Output RGB or YCbCr Shifted up 3 Bits Output RGB or YCbCr values are shifted 3 bits up. Use with R0x19B[5:4] to test LCDs with low color depth.
	2	0x0	Average Two Nearby Chrominance Bytes
	1	0x0	Swap Output Bytes In YCbCr mode, swaps chroma and Y bytes. In RGB mode, swaps odd and even bytes.
	0	0x0	Swap Red and Blue In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels.
	Output Format Control for context B. Refer to R0x13A for the corresponding control for context A.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R157:1 R0x19D	15:0	0x3CAE	Defect Correction and Noise Reduction Control (RW)
	15	0x0	Reserved.
	14	0x0	Reserved.
	13	0x1	Reduce Noise in Green 0: No green channel noise reduction. 1: Extra noise reduction in green channels.
	12	0x1	Include Center Pixel 0: Hide more defects (smooth). 1: Preserve texture.
	11	0x1	Edge Adaptive Noise Reduction 0: Hide more defects (smooth). 1: Preserve texture.
	10	0x1	Exclude Green 0: Include green in main noise reduction algorithm. 1: Exclude green in main noise reduction algorithm.
	9	0x0	Reserved.
	8	0x0	Reserved.
	7:5	0x5	Relative Threshold for Defect Correction.
	4:0	0xE	Absolute Threshold for Defect Correction.
	This register controls defect correction: R0x19D[7:0], and noise reduction: R0x19D[13:10]. Main noise reduction and green noise reduction threshold values are set in R0x147.		
R161:1 R0x1A1	10:0	0x500	Horizontal Output Size B (RW)
	Resize Context B. Must not exceed R0x1A6 Horizontal Zoom or R0x004 Column Width.		
R164:1 R0x1A4	10:0	0x400	Vertical Output Size B (RW)
	Resize Context B. Must not exceed R0x1A9 Vertical Zoom or R0x003 Row Width.		
R165:1 R0x1A5	11:0	0x4000	Horizontal Pan (RW)
	14	0x1	Origin 0: Offset from X = 0. (Left side of image.) 1: Center origin for more convenient zoom and resize.
	10:0	0x0	Horizontal Pan X Pan: Unsigned offset from X = 0 (R0x1A5[14] = 0), or two's complement from center (R0x1A5[14] = 1).
	Pan is available when the Horizontal Zoom Window is smaller than Column Width (R0x004). Adapts to sensor skip, bin and Column Width (R0x004).		
R166:1 R0x1A6	10:0	0x500	Horizontal Zoom (RW)
	Horizontal window size before reduction. Applicable to Context A and Context B. Adapts to bin, skip and sensor Column Width (R0x004). To get the largest snapshot after Automatic Zoom (R0x1AF), copy the new value from this register to the snapshot Horizontal Output Size R0x1A1 (Context B) or R0x1A7 (Context A).		
R167:1 R0x1A7	10:0	0x0280	Horizontal Output Size A (RW)
	Reducer horizontal output size in Resize context A. Must not exceed Horizontal Zoom or Sensor R0x004 Columns		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R168:1 R0x1A8	11:0	0x4000	Vertical Pan (RW)
	14	0x1	Origin 0: Origin at Y = 0. (Top) 1: Centered origin for more convenient zoom and resize.
	10:0	0x0	Vertical Pan Y Pan: unsigned offset from y = 0 (R0x1A8[14] = 0), or two's complement from center (Bit 14 = 1).
	Pan is available when Vertical Zoom is smaller than Row Width (R0x003).		
R169:1 R0x1A9	10:0	0x400	Vertical Zoom (RW)
	Reducer vertical zoom window for vertical field of view. Applicable to Context A and Context B. Use instead of Sensor Rows to avoid changing lens correction settings. Automatically adapts to Sensor Row Width changes. To get the largest snapshot after Automatic Zoom (R0x1AF) copy the new value from this register to the snapshot Horizontal Output Size R0x1A1 (context B) or R0x1A7 (context A).		
R170:1 R0x1AA	10:0	0x0200	Vertical Output Size A (RW)
	Reducer vertical output size in Resize context A. Must not exceed Vertical Zoom R0x1A9 or Sensor Row Width R0x003.		
R174:1 R0x1AE	15:0	0xC09	Reducer Zoom Step Size (RW)
	15:8	0xC	Zoom Step Size in X Recommend: 0xA: SXGA Output Size aspect ratios. 0xC: VGA Output Size aspect ratios. 0xB: CIF Output Size aspect ratios.
	7:0	0x9	Zoom Step Size in Y Recommend: 0x8: SXGA Output Size aspect ratios. 0x9: VGA Output Size aspect ratios. 0x9: CIF Output Size aspect ratios.
	Use a multiple of the Output Size aspect ratio: 5:4 for SXGA, 4:3 for VGA or 11:9 for CIF.		
R175:1 R0x1AF	15:0	0x0	Reducer Zoom Control (RW)
	14	0x0	Zoom Slow Step Zoom Window every two frames to allow Auto Exposure more time to adapt.
	12	0x0	Green Balance Compensation If R0x1AF[11] = 0 then R0x1AF[12] may be set. If R0x1AF[11] = 1 then R0x1AF[12] must be set.
	11	0x0	Binning Adjustment Enable Good for 1x to 2x reduction after binning. If R0x1AF[11] = 1, R0x1AF[12] must also be set.
	10	0x0	Reserved.
	9	0x0	Zoom Out
	8	0x0	Zoom In
	7	0x0	Reserved.
	6	0x0	Disable Integer Reducer X
	5	0x0	Disable Integer Reducer Y
	4	0x0	Reserved.
	3:0	0x0	Reserved.

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R182:1 R0x1B6	15:0	X	Lens Vertical Red Knees 6 and 5 (RW)
	15:8	X	Red Vertical Derivative Value at Vertex 6.
	7:0	X	Red Vertical Derivative Value at Vertex 5.
R183:1 R0x1B7	15:0	X	Lens Vertical Red Knees 8 and 7 (RW)
	15:8	X	Red Vertical Derivative Value at Vertex 8.
	7:0	X	Red Vertical Derivative Value at Vertex 7.
R184:1 R0x1B8	15:0	X	Lens Vertical Green Knees 6 and 5 (RW)
	15:8	X	Green Vertical Derivative Value at Vertex 6.
	7:0	X	Green Vertical Derivative Value at Vertex 5.
R185:1 R0x1B9	15:0	X	Lens Vertical Green Knees 8 and 7 (RW)
	15:8	X	Green Vertical Derivative Value at Vertex 8.
	7:0	X	Green Vertical Derivative Value at Vertex 7.
R186:1 R0x1BA	15:0	X	Lens Vertical Blue Knees 6 and 5 (RW)
	15:8	X	Blue Vertical Derivative Value at Vertex 6.
	7:0	X	Blue Vertical Derivative Value at Vertex 5.
R187:1 R0x1BB	15:0	X	Lens Vertical Blue Knees 8 and 7 (RW)
	15:8	X	Blue Vertical Derivative Value at Vertex 8.
	7:0	X	Blue Vertical Derivative Value at Vertex 7.
R188:1 R0x1BC	15:0	X	Lens Horizontal Red Knees 7 and 6 (RW)
	15:8	X	Red Horizontal Derivative Value at Vertex 7.
	7:0	X	Red Horizontal Derivative Value at Vertex 6.
R189:1 R0x1BD	15:0	X	Lens Horizontal Red Knees 9 and 8 (RW)
	15:8	X	Red Horizontal Derivative Value at Vertex 9.
	7:0	X	Red Horizontal Derivative Value at Vertex 8.
R190:1 R0x1BE	7:0	X	Lens Horizontal Red Knee 10 (RW)
	7:0	X	Red Horizontal Derivative Value at Vertex 10.
R191:1 R0x1BF	15:0	X	Lens Horizontal Green Knees 7 and 6 (RW)
	15:8	X	Green Horizontal Derivative Value at Vertex 7.
	7:0	X	Green Horizontal Derivative Value at Vertex 6.
R192:1 R0x1C0	15:0	X	Lens Horizontal Green Knees 9 and 8 (RW)
	15:8	X	Green Horizontal Derivative Value at Vertex 9.
	7:0	X	Green Horizontal Derivative Value at Vertex 8.
R193:1 R0x1C1	7:0	X	Lens Horizontal Green Knee 10 (RW)
	7:0	X	Green Horizontal Derivative Value at Vertex 10.
R194:1 R0x1C2	15:0	X	Lens Horizontal Blue Knees 7 and 6 (RW)
	15:8	X	Blue Horizontal Derivative Value at Vertex 7.
	7:0	X	Blue Horizontal Derivative Value at Vertex 6.
R195:1 R0x1C3	15:0	X	Lens Horizontal Blue Knees 9 and 8 (RW)
	15:8	X	Blue Horizontal Derivative Value at Vertex 9.
	7:0	X	Blue Horizontal Derivative Value at Vertex 8.
R196:1 R0x1C4	7:0	X	Lens Horizontal Blue Knee 10 (RW)
	7:0	X	Blue Horizontal Derivative Value at Vertex 10.

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R200:1 R0x1C8	15:0	RO	Context Control [Snooped] (RO)
	15	RO	Restart Sensor on Write.
	14	RO	Reserved.
	13	RO	Reserved.
	12	RO	Reserved.
	11	RO	Reserved.
	10	RO	Resize/Zoom Context.
	9	RO	OutputFormatCtl2Reg Context.
	8	RO	Gamma Table Context.
	7	RO	Arm Xenon Flash.
	6	RO	Blanking Control.
	5	RO	Reserved.
	4	RO	Reserved.
	3	RO	Sensor Read Mode Context [ADC2_OFF].
	2	RO	LED Flash ON.
	1	RO	Vertical Blank Select.
	0	RO	Horizontal Blank Select.
	This register returns the identical information as R0x2C8. Writes to the Page 2 version (R0x2C8) instead.		
R220:1 R0x1DC	15:0	0xE04	Gamma Table B Knee Points Y1 Y2 (RW)
	15:8	0xE	Y2
	7:0	0x4	Y1
	This register specifies output values Y1 and Y2 for the piece-wise linear gamma correction for context B. Refer to R0x153 for a description of the gamma correction table.		
R221:1 R0x1DD	15:0	0x4C28	Gamma Table B Knee Points Y3 Y4 (RW)
	15:8	0x4C	Y4
	7:0	0x28	Y3
	This register specifies output values Y3 and Y4 for the piece-wise linear gamma correction for context B. Refer to R0x153 for a description of the gamma correction table.		
R222:1 R0x1DE	15:0	0x9777	Gamma Table B Knee Points Y5 Y6 (RW)
	15:8	0x97	Y6
	7:0	0x77	Y5
	This register specifies output values Y5 and Y6 for the piece-wise linear gamma correction for context B. Refer to R0x153 for a description of the gamma correction table.		
R223:1 R0x1DF	15:0	0xC7B1	Gamma Table B Knee Points Y7 Y8 (RW)
	15:8	0xC7	Y8.
	7:0	0xB1	Y7.
	This register specifies output values Y7 and Y8 for the piece-wise linear gamma correction for context B. Refer to R0x153 for a description of the gamma correction table.		
R224:1 R0x1E0	15:0	0xEEDB	Gamma Table B Knee Points Y9 Y10 (RW)
	15:8	0xEE	Y10.
	7:0	0xDB	Y9.
	This register specifies output values Y9 and Y10 for the piece-wise linear gamma correction for context B. Refer to R0x153 for a description of the gamma correction table.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R225:1 R0x1E1	15:0	0xFF00	Gamma Table B Knee Points Y0 Y11 (RW)
	15:8	0xFF	Y11.
	7:0	0x0	Y0.
	This register specifies output values Y0 and Y11 for the piece-wise linear gamma correction for context B. Refer to R0x153 for a description of the gamma correction table.		
R226:1 R0x1E2	10:0	0x7000	Effects Mode (RW)
	15:8	0x70	Solarization Threshold. Provides the threshold for the solarization effects.
	2:0	0x0	Effects Mode. Selects the desired effect: 000: No effect. 001: Monochrome. 010: Sepia. 011: Negative. 100: Solarization 1. 101: Solarization 2. 110: Reserved. 111: Reserved.
	This register controls the special effects unit.		

Table 16: Page 1: Image Processing Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg. # Decimal Hex	Bits	Default	Description
R227:1 R0x1E3	15:0	0xB023	Effects Sepia Color (RW)
	15	0x1	Cb Sign.
	14:8	0x30	Cb Magnitude.
	7	0x0	Cr Sign.
	6:0	0x23	Cr Magnitude.
	This register provides the chroma values for the Sepia effect.		
R240:1 R0x1F0	2:0	0x0	Page Map (RW)
	2:0	0x0	Page Address: 000: Sensor address page. 001: Colorpipe Address page. 010: Camera control address page. 011–111: Reserved.
	This register specifies the memory address page for the two-wire interface protocol.		
R241:1 R0x1F1	15:0	0x0	Byte Wise Address (RW)
	Use this register to perform reads and writes to the sensor in two 8-bit serial transmissions instead of one 16-bit.		

Page 2: Camera Control Register Descriptions

Table 17: Page 2: Camera Control Register Descriptions
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R2:2 R0x202	8:0	0xEE	Base Matrix Signs (RW)
	8	0x0	Sign of K1 The sign of K1 is always positive; therefore, this bit is always "0."
	7	0x1	Sign of K2.
	6	0x1	Sign of K3.
	5	0x1	Sign of K4.
	4	0x0	K5 always positive. The sign of K5 is always positive; therefore, this bit is always "0."
	3	0x1	Sign of K6.
	2	0x1	Sign of K7.
	1	0x1	Sign of K8.
	0	0x0	K9 always positive The sign of K9 is always positive; therefore, this bit is always "0."
	This register specifies the signs of the nine coefficients in the base color correction matrix. Refer to the description of R0x209 for a detailed description of the base and delta color correction matrices.		
R3:2 R0x203	14:0	0x2923	Base Matrix Scale K1- K5 (RW)
	14:12	0x2	Scaling of K5.
	11:9	0x4	Scaling of K4.
	8:6	0x4	Scaling of K3.
	5:3	0x4	Scaling of K2.
	2:0	0x3	Scaling of K1.
	This register specifies the scaling of coefficients K1 through K5 of the color correction matrices. Refer to the description of R0x209 for a detailed description of the color correction matrices. The magnitudes of all coefficients are stored as 8-bit unsigned integers. The scaling scheme accommodates fractional coefficient magnitudes in the range from 0.004 through 15.93. Prior to loading, fractional coefficients are multiplied by 16, 32, 64, 128, or 256 and rounded to the nearest integer. For maximum accuracy, the scale factor should be selected so that the scaled coefficient is as close as possible to, but not exceeding, 255. The power of 2 used for scaling in excess of 4 is specified as a 3-bit value in R0x203 and R0x204. The encoding is: 000: Scale by 16. 001: Scale by 32. 010: Scale by 64. 011: Scale by 128. 100: Scale by 256. 101: Reserved. 110: Reserved. 111: Reserved. A single scale factor is used for the corresponding coefficients in the base and delta matrices.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R4:2 R0x204	11:0	0x4E4	Base Matrix Scale K6 - K9 (RW)
	11:9	0x2	Scaling of K9.
	8:6	0x3	Scaling of K8.
	5:3	0x4	Scaling of K7.
	2:0	0x4	Scaling of K6.
	This register specifies the scaling of color correction coefficients K6 through K9 of the color correction matrices. Refer to R0x203 for more details.		
R6:2 R0x206	15:0	0x600E	Mode Control [Snooped] (RW)
	15	0x0	Manual White Balance
	14	0x1	Auto Exposure
	13	0x1	Defect Correction
	12	0x0	Aperture Correction
	11	0x0	AWB Matrix Control
	10	0x0	Lens Shading Correction
	9	0x0	Reserved.
	8	0x0	Reserved.
	7	0x0	Auto Flicker Detection
	6	0x0	Reserved.
	5	0x0	Reserved.
	4	0x0	Bypass Color Processing
	3:2	0x3	Auto Exposure Window Ctrl - Backlight compensation
	1	0x1	AWB Control
	0	0x0	Unused
	This register returns the identical information as R0x106. Writes to the Page 2 version (R0x106) instead.		
R9:2 R0x209	7:0	0xD0	Base Matrix Coefficient K1 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K1. The AWB algorithm selects the appropriate intermediate point between 2 color correction matrices calibrated at the "edges" of the expected spectra of illumination (for example, blue-rich sunlight and red-rich incandescent light). The mid-point between the two “extremum” matrices is the base matrix, and the difference between them is the delta matrix. Scaled magnitudes of the coefficients of the base matrix (K1 through K9) are programmed in registers R0x209 through R0x211. The scaling scheme is described in R0x203. It is important that scaling ensures that neither the base nor the delta matrix overflows. As with the color correction matrix, AWB also interpolates sensor gain ratios from which it derives Imager Core gain settings to obtain better SNR. These ratios correspond to matrix positions and are described in R0x25E.		
R10:2 R0x20A	7:0	0x52	Base Matrix Coefficient K2 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K2. Refer to R0x209 for more details.		
R11:2 R0x20B	7:0	0x4	Base Matrix Coefficient K3 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K3. Refer to R0x209 for more details.		
R12:2 R0x20C	7:0	0x94	Base Matrix Coefficient K4 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K4. Refer to R0x209 for more details.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R13:2 R0x20D	7:0	0x82	Base Matrix Coefficient K5 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K5. Refer to R0x209 for more details.		
R14:2 R0x20E	7:0	0x3F	Base Matrix Coefficient K6 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K6. Refer to R0x209 for more details.		
R15:2 R0x20F	7:0	0x60	Base Matrix Coefficient K7 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K7. Refer to R0x209 for more details.		
R16:2 R0x210	7:0	0x9C	Base Matrix Coefficient K8 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K8. Refer to R0x209 for more details.		
R17:2 R0x211	7:0	0xB6	Base Matrix Coefficient K9 (RW)
	This register specifies the scaled magnitude of the base color correction matrix coefficient K9. Refer to R0x209 for more details.		
R18:2 R0x212	6:0	RO	AWB Position (RO)
	This register specifies the current position of the color correction matrix relative to the original calibration matrices. The matrix position is expressed as a 7-bit number represented in 0.bbbbbbb fixed point. Positions range from 0/128 for red-rich illumination to 127/128 for blue-rich illumination.		
R19:2 R0x213	7:0	RO	AWB Red Digital Gain (RO)
	This register reports the current value of the red digital gain as an 8-bit number in b.bbbbbbb fixed point, which ranges from 0/128 to 255/128.		
R20:2 R0x214	7:0	RO	AWB Blue Digital Gain (RO)
	This register reports the current value of the blue digital gain as an 8-bit number in b.bbbbbbb fixed point, which ranges from 0/128 to 255/128.		
R21:2 R0x215	8:0	0xC9	Delta Coefficients Signs (RW)
	8	0x0	Sign of D1.
	7	0x1	Sign of D2.
	6	0x1	Sign of D3.
	5	0x0	Sign of D4.
	4	0x0	Sign of D5.
	3	0x1	Sign of D6.
	2	0x0	Sign of D7.
	1	0x0	Sign of D8.
	0	0x1	Sign of D9.
	This register specifies the signs of the 9 coefficients of the delta color correction matrix. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R22:2 R0x216	7:0	0x5D	Delta Matrix Coefficient D1 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D1. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R23:2 R0x217	7:0	0x9C	Delta Matrix Coefficient D2 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D2. Refer to the description of R0x209 for a detailed description of the color correction matrices.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R24:2 R0x218	7:0	0x3	Delta Matrix Coefficient D3 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D3. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R25:2 R0x219	7:0	0x44	Delta Matrix Coefficient D4 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D4. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R26:2 R0x21A	7:0	0x9	Delta Matrix Coefficient D5 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D5. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R27:2 R0x21B	7:0	0x50	Delta Matrix Coefficient D6 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D6. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R28:2 R0x21C	7:0	0x71	Delta Matrix Coefficient D7 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D7. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R29:2 R0x21D	7:0	0x79	Delta Matrix Coefficient D8 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D8. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R30:2 R0x21E	7:0	0x63	Delta Matrix Coefficient D9 (RW)
	This register specifies the scaled magnitude of the delta color correction matrix coefficient D9. Refer to the description of R0x209 for a detailed description of the color correction matrices.		
R31:2 R0x21F	8:0	0x0180	White Balance Cb and Cr Limits (RW)
	8:6	0x6	Relative Limit Relative test, which compares the magnitudes of the 7-bit chromas to the largest 8-bit RGB component (= max_color) for the pixel: 000: No pixels passes the test. 001: Chromas less than 1/8 max_color pass the test. 010: Chromas less than 1/4 max_color pass the test. 011: Chromas less than 3/8 max_color pass the test. 100: Chromas less than 1/2 max_color pass the test. 101: Chromas less than 5/8 max_color pass the test. 110: Chromas less than 3/4 max_color pass the test. 111: Chromas less than 7/8 max_color (nearly all pixels) pass the test.
	5:0	0x0	Absolute Limit Absolute test: Chromas must both lie below this value
	This register controls chroma tests that prevent deeply saturated colors from skewing the White Balance statistics. Pixels that fail these tests are not counted.		
R32:2 R0x220	15:0	0xC814	Luminance Limits for White Balance Statistics (RW)
	15:8	0xC8	Upper Limit Upper limit of luminance for White Balance statistics.
	7:0	0x14	Lower Limit Lower limit of luminance for White Balance statistics.
	To avoid skewing White Balance statistics by very dark or very bright values, this register represents the luminance range of pixels to be used for White Balance statistics. These limits are 8-bit values represented as 0.bbbbbbbb fixed point in the range of 0/256 to 224/256.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R33:2 R0x221	15:0	0x8080	Red Blue Gain for Manual White Balance (RW)
	15:8	0x80	Red Gain Red channel gain.
	7:0	0x80	Blue Gain Blue channel gain.
	This register stores the red and blue color channel gains for use when manual white balance is enabled (R0x106[15] = 1). The programmed values represent the desired gains as 8-bit numbers in b.bbbbbbb fixed point, which range from 0/128 to 255/128. As an example, unity gain has the value 0x80.		
R34:2 R0x222	15:0	0x9080	AWB Red Limit (RW)
	15:8	0x90	Upper Limit Upper limit of red channel gain.
	7:0	0x80	Lower Limit Lower limit of red channel gain.
	This register sets the range of red gain adjustment by the AWB algorithm. To preserve full-range red, a lower limit below 0.75 is not recommended when using default matrices. The 8-bit gain limits are represented in b.bbbbbbb fixed point. Values range from 0/128 to 255/128.		
R35:2 R0x223	15:0	0x8878	AWB Blue Limit (RW)
	15:8	0x88	Upper Limit Upper limit of blue channel gain.
	7:0	0x78	Lower Limit Lower limit of blue channel gain.
	This register sets the range of blue gain adjustment by the AWB algorithm. To preserve full-range blue, a lower limit below 0.75 is not recommended when using default matrices. The 8-bit gain limits are represented in b.bbbbbbb fixed point. Values range from 0/128 to 255/128.		
R36:2 R0x224	15:0	0x7F00	Matrix Adjustment Limits (RW)
	15	0x0	Reserved.
	14:8	0x7F	Upper Limit Upper limit of the matrix position.
	7	0x0	Reserved.
	6:0	0x0	Lower Limit Lower limit of the matrix position.
	As described in R0x212, AWB determines the best position of the color correction matrix by interpolating between 2 "edge" matrices: one for red-rich illumination and one for blue-rich illumination. The limits of the matrix position are expressed as 7-bit numbers represented in 0.bbbbbbb fixed point. Positions range from 0/128 for red-rich illumination to 127/128 for blue-rich illumination.		
R38:2 R0x226	15:0	0x8000	Auto Exposure Full Window Horizontal Boundaries (RW)
	15:8	0x80	Right Boundary
	7:0	0x0	Left Boundary
	This register specifies the left and right boundaries of the full window used by the Auto Exposure measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 (decimal) is the left-most edge of the frame.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R39:2 R0x227	15:0	0x8008	Auto Exposure Full Window Vertical Boundaries (RW)
	15:8	0x80	Bottom Boundary
	7:0	0x8	Top Boundary
	This register specifies the top and bottom boundaries of the full window used by the Auto Exposure measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 (decimal) is the topmost edge of the frame.		
R40:2 R0x228	15:0	0xEA02	AWB Advanced Control
	15	0x1	Reserved.
	14	0x1	Reserved.
	13	0x1	Reserved.
	12	0x0	AWB Load Color Correction Parameters Control This register is set by user after programming the Color Correction registers. This auto reset bit is cleared when the matrix interpolation is done.
	11	0x1	Reserved.
	10	0x0	Reserved.
	9:8	0x2	Reserved.
	6:3	0x0	Matrix Adjustment Frequency Specifies the frequency of matrix adjustments. The color correction matrix is adjusted once in N frames, where N is the value of this field.
	2:0	0x2	Gain Adjustment Smoothing Specifies the amount of smoothing of gain adjustments: 000: current gain = new gain. 001: current gain = 1/2 new gain + 1/2 old gain. 010: current gain = 1/4 new gain + 3/4 old gain. 011: current gain = 1/8 new gain + 7/8 old gain. 100: current gain = 1/16 new gain + 15/16 old gain. 101: current gain = 1/32 new gain + 31/32 old gain. 110: current gain = 1/64 new gain + 63/64 old gain. 111: current gain = 1/128 new gain + 127/128 old gain.
R41:2 R0x229	15:0	0x867A	Wide AWB Gates (RW)
	15:8	0x86	Upper Limit
	7:0	0x7A	Lower Limit
	This register describes the hysteresis window for AWB matrix motion. The 8-bit fields contain values in b.bbbbbbb fixed point, which represent numbers from 0/128 to 255/128. Whenever the blue digital gain lies outside this window, it triggers AWB to move the color correction matrix toward a position with the blue digital gain near unity.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R42:2 R0x22A	15:0	0xD0	Standard Deviation Limits for a Monochrome Zone (RW)
	15:8	0x0	Minimum Number of Zones for White Balance Statistics Minimum number of zones that must be valid for the set of regions of interest to be considered valid.
	7:4	0xD	Upper Limit of Standard Deviation Upper bound on the hue variation threshold.
	3:0	0x0	Lower Limit of Standard Deviation Lower bound on the hue variation threshold.
	This register contains three parameters used in the white balance calculation to select regions of interest. The hue variation threshold parameters bound the range within which the hue variation threshold can wander as it attempts to keep the number of valid regions of interest (zones) close to, but above, the minimum number of regions of interest specified in the third parameter. This behavior attempts to keep the white balance algorithm focused on the most useful regions of the image while ignoring those that might imbalance the statistics.		
R43:2 R0x22B	15:0	0x6020	Auto Exposure Center Window Horizontal Boundaries (RW)
	15:8	0x60	Right Boundary Right window boundary.
	7:0	0x20	Left Boundary Left window boundary.
	This register specifies the left and right boundaries of the center window used by the Auto Exposure measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 (decimal) is the left most edge of the frame.		
R44:2 R0x22C	15:0	0x6020	Auto Exposure Center Window Vertical Boundaries (RW)
	15:8	0x60	Bottom Boundary Bottom window boundary.
	7:0	0x20	Top Boundary Top window boundary.
	This register specifies the top and bottom boundaries of the center window used by the Auto Exposure measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottommost edge of the frame, 64 (decimal) is the middle of the frame, and 0 (decimal) is the topmost edge of the frame.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R45:2 R0x22D	15:0	0xF0A0	Boundaries for White Balance Window (RW)
	15:12	0xF	Bottom Boundary Bottom window boundary (in units of blocks).
	11:8	0x0	Top Boundary Top window boundary (in units of blocks).
	7:4	0xA	Right Boundary Right window boundary (in units of 2 blocks).
	3:0	0x0	Left Boundary Left window boundary (in units of 2 blocks).
	This register specifies the boundaries of the window used by the White Balance measurement engine. It describes the window in terms relative to the size of the image: horizontally, in units of 1/10 of the width of the image; vertically, in units of 1/16 of the height of the image. Although the positioning is highly quantized, the window remains roughly in place as the resolution changes. More precisely, the values in the registers are the desired boundaries, in units of square blocks of pixels vertically, and in units of two such blocks horizontally. The size of the blocks is determined by the resolution of the image seen by the White Balance measurement engine and is 8 x 8, 16 x 16, 32 x 32, or 64 x 64 pixels. The block size is the smallest size that can cover the image with no more than 20 blocks horizontally and 16 blocks vertically. Using this concept of blocks, the window scales as the image size changes, albeit coarsely. Care must be taken when the aspect ratio of the image deviates substantially from that of a full-resolution image, as the horizontal and vertical dimensions suggest very different choices of block size. When this happens, the larger block size is selected, leading to greater quantization along one dimension.		
R46:2 R0x22E	15:0	0xC44	Auto Exposure Target and Precision Control (RW)
	15:8	0xC	Auto Exposure Hysteresis Window. Half-size of the Auto Exposure target luma stability window.
	7:0	0x44	Static Target Luma Value. Luma value of the Auto Exposure static target.
	This register specifies the luma target of the auto exposure algorithm and the size of the window/range around the target in which no Auto Exposure adjustment is made. This window is centered on target, but the value programmed in the register is 1/2 of the window size. R0x22E[7:0] have a range of [0–224]. This is target luma that Auto Exposure is attempting to achieve. R0x22E[15:8] is the half-width of the window around the target luma that provides hysteresis, that is, Auto Exposure is considered adapted if the time averaged luma (R0x24D) is equal to the value in R0x22E[7:0] + or - R0x22E[15:8]. Make sure that (R0x22E[7:0] – R0x22E[15:8]) remains nonnegative.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R47:2 R0x22F	15:0	0x9120	Auto Exposure Speed and Sensitivity Control A (RW)
	15	0x1	Auto Exposure Integration Change Decision Delay Delays the next Auto Exposure decision by a frame when the shutter width has changed.
	14	0x0	Auto Exposure Saturated Pixel Adaption Enable Enables Auto Exposure algorithm to boost effort when saturated pixels are present. When a substantial number of saturated pixels are present, the ability to correctly estimate exposures based upon current luminance is reduced.
	13:12	0x1	Auto Exposure Saturated Pixel Adaption Strength Controls how much boost the Auto Exposure algorithm gets when the frame is dominated by saturated pixels. When the saturated pixel measurement indicates that so many pixels are saturated that the target luminance is unreachable through a linear exposure estimate, there is a division by zero condition. This field limits how close to zero the denominator of the Auto Exposure estimate can approach. The value is a power of two, where larger values result in a denominator closer to zero, which in turn results in a larger exposure setting change.
	11	0x0	Reserved.
	10	0x0	Reserved.
	9	0x0	Reserved.
	8:6	0x4	Auto Exposure Adaption Speed Factor of reduction of the difference between current luma and target luma. In one adjustment Auto Exposure advances from current luma to target as follows: 000: 1/4 way going down, 1/8 going up. 001: 1/4 way in both directions. 010: 1/2 way in both directions. 011: 1/2 way going down, 1/4 going up. 100: All the way in both directions (fast adaption). 101: 3/4 way in both directions. 110: 7/8 way in both directions. 111: Reserved.
	5	0x1	Auto Exposure Dynamic Target Enable Dynamic Target Auto Exposure algorithm. If enabled, R0x22F[14] must be set to zero for algorithm stability.
	4:3	0x0	Auto Exposure Decision Frequency Exposure is evaluated every N + 1 frames, where N is given by this field.
	2:0	0x0	Auto Exposure Luma Hysteresis Hysteresis control through time-averaged smoothing of luma data. Luma measurements for Auto Exposure are time-averaged as follows: 000: Auto Exposure luma = current luma. 001: Auto Exposure luma = 1/2 current luma + 1/2 buffered value. 010: Auto Exposure luma = 1/4 current luma + 3/4 buffered value. 011: Auto Exposure luma = 1/8 current luma + 7/8 buffered value. 100: Auto Exposure luma = 1/16 current luma + 15/16 buffered value. 101: Auto Exposure luma = 1/32 current luma + 31/32 buffered value. 110: Auto Exposure luma = 1/64 current luma + 63/64 buffered value. 111: Auto Exposure luma = 1/128 current luma + 127/128 buffered value.
	This register specifies Auto Exposure speed and sensitivity to changes for context A. Refer to register R0x29C for the context B version.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R48:2 R0x230	7:0	RO	Red White Balance Measurement (RO)
	This register outputs the White Balance measurement of red in the image. This value is normalized to an arbitrary value that is the same for R0x230, R0x231, and R0x232. Only the ratios between these registers are meaningful.		
R49:2 R0x231	7:0	RO	Luma White Balance Measurement (RO)
	This register outputs the White Balance measurement of luminance in the image. This value is normalized to an arbitrary value that is the same for R0x230, R0x231, and R0x232. Only the ratios between these registers are meaningful.		
R50:2 R0x232	7:0	RO	Blue White Balance Measurement (RO)
	This register outputs the White Balance measurement of blue in the image. This value is normalized to an arbitrary value that is the same for R0x230, R0x231, and R0x232. Only the ratios between these registers are meaningful.		
R51:2 R0x233	15:0	0x146E	Sharpness and Saturation Control (RW)
	15:8	0x14	75% to 50% Threshold to reduce saturation and sharpness to 50%.
	7:0	0x6E	100% to 75% Threshold to reduce saturation and sharpness to 75%.
	This register specifies the Auto Exposure thresholds at which sharpness (aperture correction) and color saturation are automatically reduced. This reduction leads to lower image noise at high gain settings (low-light scenes). There are two gain thresholds at which sharpness and color saturation are reduced, first to 75%, and then to 50% of their full values. The automatic control of sharpness is enabled by setting R0x105[3], and automatic control of color saturation is enabled by setting R0x23E[12]. Sharpness is never made higher than the originally programmed settings. The thresholds are programmed in terms of values from 1 to 255 and are compared with the current imager core gain, ADC gain, or digital gains (refer to R0x23E).		
R53:2 R0x235	15:0	0xB010	Dynamic Target Luma (RW)
	15:8	0xB0	Upper bound limit of Dynamic Target Luma
	7:0	0x10	Lower bound limit of Dynamic Target Luma
	This registers sets the lower and upper bounds on the dynamic target luma. The range of each of these bounds is in the interval of [0–224]. The lower bound must not be greater than the upper bound, and the upper bound must be set below 190, for exposure stability.		
R54:2 R0x236	15:0	0x7810	Auto Exposure Gain Limits (RW)
	15:8	0x78	Upper Limit Upper gain limit. The 8-bit value is in bbbb.bbbb fixed point format. The nominal value is about 1/2 the maximum possible analog gain.
	7:0	0x10	Lower Limit. Lower gain limit. The 8-bit value is in bbbb.bbbb fixed point format. The nominal value is 1.0 (0x10).
	This register specifies upper and lower virtual analog gain limits for the Auto Exposure algorithm. The physical red and blue analog gains are derived using the analog gain ratios supplied by AWB. Any changes to the fields of this register must be coordinated with the values of the Auto Exposure gain zone table (R0x282–R0x295).		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R55:2 R0x237	15:0	0x300	Auto Exposure Gain Zone Limits (RW)
	15	0x0	Force Auto Exposure Settings Reevaluation When set, forces Auto Exposure to reevaluate its exposure settings considering any new limits or parameters. This bit auto-clears after the new settings become active.
	9:5	0x18	Upper Gain Zone Limit Highest zone number allowed for shutter width adjustment. Highest gain zone permitted. The range is [0–24]. Changing this field value initiates a shift between day mode and night mode exposure settings. The day and night mode gain zone settings are listed in R0x281. When transitioning between day and night mode, set R0x237[15] of this register to force Auto Exposure to recalculate its exposure settings.
	4:0	0x0	Lower Gain Zone Limit Lowest gain zone permitted. The range is [0–24]. Since a good deal of exposure dynamic range is contained in zone 0, this value should almost always be set to 0.
	This register (R0x237) sets upper and lower limits on the Auto Exposure zones, and by extension, the limits on available shutter widths. The gain zone table (R0x282–R0x295) is used to establish a bounded range of gains that can be assumed within each zone. Each zone (except for zone 0) is an integral multiple of the “flicker period,” which is usually the inverse of twice the AC power line frequency. This is the period of time over which the exposure should integrated, to avoid artifacts from the periodic nature of fluorescent and incandescent lighting. The zones range from 0 to 24, with zone 0 being Reserved for shutter widths less than the flicker period. All shutter widths that can be used by the Auto Exposure module are assigned to the 25 zones of the exposure gain table as follows (assuming 30 fps frame rate, 60Hz power line frequency): Zone 0 includes shutter widths from 8 line times up to a 1/4 of a full frame (where full frame is the number of active lines plus the number of vertical blanking rows). Zone 1 is exactly 1/4 of the full frame time. Zones 2 through 24 correspond to shutter widths increasing in 1/4 frame increments up to 6 full frames (corresponding to 1/5 sec.). Within the Zones bounded by this register (except the last Zone), the permissible gains are limited by the exposure table. For 15 fps, the frame fraction is halved from 1/4 to 1/8. For 50Hz power line frequency, the frame rate is either 25 fps or 12.5 fps, and Zone 24 corresponds to 6/25 of a second. By default, Auto Exposure favors exposure time increases over gain increases. For the last Zone, which can be set to less than 24 by the highest zone number limit of this register, Auto Exposure permits gains which are only bounded by the Auto Exposure Gain Limits register.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R56:2 R0x238	11:0	0x440	Auto Exposure Gain Table Range Control (RW)
	11:8	0x4	Mid-Range Gain Zone Lowest gain zone to favor gain over increase in shutter width. If this value is 11 or greater, all zones within the range limits imposed by R0x237 favor shutter width over gain.
	7:0	0x40	Mid-Range Gain Limit Upper virtual gain limit in zones R0x238[11:8] to R0x237[9:5]. After zone R0x237[9:5], it is superseded by the Upper gain limit specified in R0x236[15:8].
	To achieve the required amount of exposure the auto exposure algorithm adjusts the sensor exposure time (shutter width, R0x009; shutter delay, R0x00C) and gains (R0x02B - R0x02E; R0x041). For any given exposure, the best signal-to-noise ratio can be typically obtained by using the longest exposure and the smallest gain setting. However, a long exposure time can slow down the output frame rate if the former exceeds the default frame rate (shutter width > image height + vertical blank). R0x238[11:8] specifies the break point where the scheme of preferential increase of shutter width is replaced with the scheme of preferential increase in gain. R0x238[11:8] splits the gain lookup table R0x282–R0x295 into two parts. Entries in the first part, zones 0 to (R0x238[11:8] - 1), specify maximum gain values, with the minimum gain being given by R0x236[7:0]. The maximum values are precalculated such that the internal auto exposure calculation loop, when transitioning between gain zones, establishes a combined change to exposure (shutter width and gain change) such that the resultant image luminance changes by 1/16. Within gain zones 1 through 24, the gains are also stepped in increments of 1/16 between the minimum and maximum bounds. The second part of the gain table, from gain zone R0x238[11:8] to gain zone 11, specifies minimum gains, with the maximum gain being given by R0x238[7:0]. The minimum gain presets are calculated with the same 1/16 exposure increment goal between zone transitions as the maximum gain presets in the first part of the table. When the current zone reaches R0x237[9:5] (the upper gain zone limit), the gain maximum is then governed by R0x236[15:8] (the upper gain limit).		
R57:2 R0x239	10:0	0x690	Auto Exposure Line Size A (RW)
	Total number of pixels in a row including horizontal blanking in context A.		
R58:2 R0x23A	10:0	0x626	Auto Exposure Line Size B (RW)
	Total number of pixels in a row including horizontal blanking in context B.		
R59:2 R0x23B	10:0	0x3DE	Auto Exposure Shutter Delay Limit A (RW)
	Maximum shutter delay for context A. Values for shutter delay computed by Auto Exposure will be clamped to this value.		
R60:2 R0x23C	10:0	0x4CA	Auto Exposure Shutter Delay Limit B (RW)
	Maximum shutter delay for context B. Values for shutter delay computed by Auto Exposure will be clamped to this value.		
R61:2 R0x23D	13:0	0x18DD	Auto Exposure ADC Adjustment Limits (RW)
	13	0x0	Reserved.
	12	0x1	Reserved.
	11:8	0x8	Lower VREFLO Limit Minimum limit value for VREFLO.
	7:4	0xD	Upper VREFHI Limit Maximum limit value for VREFHI.
	3:0	0xD	Lower VREFHI Limit Minimum limit value for VREFHI.
	The sensor ADC VREFLO and VREFHI values can be manipulated by the Auto Exposure algorithm to achieve additional analog gain. Up to a factor of 3X additional gain is possible, although no more than 2X is recommended.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R62:2 R0x23E	12:0	0x1CFF	Gain Threshold for CCM Adjustment (RW)
	12	0x1	Automatic Saturation Control Enable Automatic color saturation control. 0: Disable automatic color saturation control 1: Enables automatic color saturation control as specified here and in R0x233. The automatic saturation control is independent of the saturation adjustments specified in the R0x125.
	11:10	0x3	Gain Type for Saturation Control 50% Threshold Select gain type for automatic saturation control 50% threshold. Refer to R0x233[15:8]. 00: Virtual analog gain. 01: ADC VREFLO. 10: Digital gain. 11: LC digital gain.
	9:8	0x0	Gain Type for Saturation Control 75% Threshold Select gain type for automatic saturation control 75% threshold. Refer to R0x233[7:0]. 00: Virtual analog gain. 01: ADC VREFLO. 10: Digital gain. 11: LC digital gain.
	7:0	0xFF	Threshold to Disable CCM in Dark Gain threshold to disable Color Correction Matrix adjustment at high virtual gains, which imply low light.
	This register contains the selection of gain sources for the automatic saturation control and the virtual gain threshold at which Color Correction Matrix adjustment is disabled.		
R63:2 R0x23F	4:0	RO	Auto Exposure Zone Index (RO)
	This register monitors the current value of the index to the exposure gains table. A zone of 0 indicates a bright image, with shutter widths set without regard to flicker abatement. Zones 1-4 reflect shutter widths that permit full frame rate. Zones 5-24 reflect increasing integration times, with a corresponding decrease in frame rate governed by the inclusive limits set in R0x236.		
R70:2 R0x246	7:0	0x0	Auto Exposure Zone 0 Luma Threshold (RW)
	In bright indoor conditions (where flicker may be present), this threshold helps delay the reduction of integration time below Auto Exposure gain zone 1. When in Auto Exposure gain zone 1, the current luma value is permitted to rise to a value specified in this register, which can be higher than that specified by the target luma R0x22E[7:0]. This helps forestall the appearance of flicker in the image, but the image may become overexposed. A value of "0" disables this functionality.		
R76:2 R0x24C	15:0	RO	Auto Exposure Current Measured Luma (RO)
	The value of this register is the normalized sum of pre-gamma corrected luma samples, as determined by the Auto Exposure backlight compensation field of the Mode Control Register (R0x106[3:2]). The format of this register is fixed point bbbbbbbb.bbbbbbbb, with a range of [0.0–224.0].		
R77:2 R0x24D	7:0	RO	Auto Exposure Time Averaged Luma (RO)
	The value of this register is the time-averaged normalized sum of all the pre-gamma corrected luma samples (time-averaged luma), as determined by the Auto Exposure backlight compensation field of the Mode Control Register (R0x106[3:2]). However, when the time-averaged luma moves outside the luma target range, the time averaging is disabled and this registers value becomes identical to that of R0x24C[15:9].		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R87:2 R0x257	11:0	0x1DC	Shutter Width Basis 60Hz A (RW)
	Number of shutter width rows to yield an integration time of 1/30 of a second (for 60Hz flicker setting for Auto Exposure Gain Zone 4). Context A.		
R88:2 R0x258	11:0	0x23B	Shutter Width Basis 50Hz A (RW)
	Number of shutter width rows to yield an integration time of 1/25 of a second (50Hz flicker setting for Auto Exposure Gain Zone 4). Context A.		
R89:2 R0x259	11:0	0x1FC	Shutter Width Basis 60Hz B (RW)
	Number of shutter width rows to yield an integration time of 1/30 of a second (for 60Hz flicker setting for Auto Exposure gain zone 4). Context B.		
R90:2 R0x25A	11:0	0x261	Shutter Width Basis 50Hz B (RW)
	Number of shutter width rows to yield an integration time of 1/25 of a second (for 50Hz flicker setting for Auto Exposure gain table zone 4). Context B.		
R91:2 R0x25B	6:0	0x2	Flicker Control (RW)
	15	0x0	Detect 60Hz output (read only) 50/60Hz detected. 0: 50Hz. 1: 60Hz.
	2	0x0	Skip frame Skip frame before processing next two frames.
	1	0x1	Manual 50/60 When in “manual” flicker mode (R0x25B[0] = 1), defines which flicker frequency to avoid. 0: 50Hz. 1: 60Hz.
	0	0x0	Flicker detection mode 0: Auto flicker detection. 1: Manual Mode.
	Primary flicker control register.		
R92:2 R0x25C	15:0	0x110C	Search flicker 60Hz (RW)
	15:8	0x11	Max search flicker period Max search flicker period for 60Hz.
	7:0	0x0C	Min search flicker period Min search flicker period for 60Hz.
	A key aspect of the flicker detection algorithm is the search for a sine wave in a buffer of stored luma values. When a sine wave is detected, the number of samples that constitute a cycle is compared to a search range for 60Hz flicker and one for 50Hz flicker. R0x25C and R0x25D define these search ranges. The middle of the range (or expected number of samples per sine wave) is calculated as: N = (1/2 * flicker- freq) / 8 * (line-time). For 60Hz, N = (1/120) / (8 * line-time). The line-time is simply: (Active Cols + HBlank) / (Sensor pixel clock period). Contact your local FAE for spreadsheet to calculate these values. R0x0x25C[7:0] is typically set to N - 3 or the midway point between the 60Hz flicker search range center and the 50Hz flicker search range center. R0x25C[15:8] is typically set to N + 3.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R93:2 R0x25D	15:0	0x1510	Search flicker 50Hz (RW)
	15:8	0x15	Max search flicker period Man search flicker period for 50Hz.
	7:0	0x10	Min search flicker period Min search flicker period for 50Hz.
	Flicker search range for 50Hz. Refer to R0x25C for details.		
R94:2 R0x25E	15:0	0x5848	Ratios of Imager Gains - Base (RW)
	15:8	0x58	Base Blue/Green Gain Ratio Base Blue/Green Ratio = (BlueGain/GreenGain (right) + BlueGain/GreenGain (left)) / 2.
	7:0	0x48	Base Red/Green Gain Ratio Base Red/Green Ratio = (RedGain/GreenGain (right) + RedGain/GreenGain (left)) / 2.
	This register specifies the magnitudes of the base imager core analog gain ratios used during the calibration of the edge color correction matrices. As with the color correction matrix coefficients, the base ratios are the average of the ratios at the extreme calibration points. They are 8-bit numbers represented in bb.bbbbbb fixed point, and they are always positive.		
R95:2 R0x25F	15:0	0x2021	Ratios of Imager Gains - Delta (RW)
	15:8	0x20	Delta Blue/Green Gain Ratio Delta Blue/Green Ratio = BlueGain/GreenGain (right) - BlueGain/GreenGain (left).
	7:0	0x21	Delta Red/Green Gain Ratio Delta Red/Green Ratio = RedGain/GreenGain (right) - RedGain/GreenGain (left).
	This register specifies the magnitudes of the imager core analog gain ratio deltas derived from the calibration of the "edge" color correction matrices. As with the color correction matrix coefficients, the gain ratio deltas are the differences between the sensor gain ratios at the blue-rich and red-rich extreme calibration points. They are 8-bit numbers represented in bb.bbbbbb fixed point, and their signs are stored in R0x260.		
R96:2 R0x260	1:0	0x2	Ratios of Imager Gains - Delta Signs (RW)
	1	0x1	Sign of Delta Blue/Green Gain Ratio Sign of the delta of the blue/green imager core analog gain ratio.
	0	0x0	Sign of Delta Red/Green Gain Ratio Sign of the delta of the red/green imager core analog gain ratios.
	This register specifies the signs of the deltas of the imager core analog gain ratio.		
R97:2 R0x261	15:0	RO	AWB Analog Gain Ratios Monitor (RO)
	15:8	RO	Blue/Green Gain Ratio Monitor Sensor analog gain ratio for blue/green.
	7:0	RO	Red/Green Gain Ratio Monitor Sensor analog gain ratio for red/green.
	This register reflects the current values of the sensor analog gain ratios computed by the AWB unit.		
R98:2 R0x262	15:0	0x1010	Auto Exposure Digital Gains (RW)
	15:8	0x10	Post Lens Correction Digital Gain Post Lens correction Digital Gain (writable if Auto Exposure is disabled).
	7:0	0x10	Pre Lens Correction Digital Gain Pre Lens Correction Digital Gain (writable if Auto Exposure is disabled).
	These digital gains are applied within the IFP; they are independent of the Imager gains. Writable only when Auto Exposure is disabled, R0x106[14] = 0.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R101:2 R0x265	9:0	0x0	Auto Exposure Luma Measurement Offset (RW)
	This value is subtracted from all the pixel values that contribute to current luma (and time-averaged luma). The resultant value is clamped at "0." The default value of this register should be at least the default value of colorpipe register R0x13C[9:0], if R0x13C[10] is set.		
R103:2 R0x267	15:0	0x2010	Auto Exposure Digital Gain Limits (RW)
	15:8	0x20	Post-Lens Correction Digital Gain Upper Limit Maximum limit on post-lens correction digital gain.
	7:0	0x10	Pre-Lens Correction Digital Gain Upper Limit Maximum limit on pre-lens correction digital gain.
	This register specifies the upper limits of the digital gains used by the Auto Exposure algorithm. The values programmed into this register are in fixed point bbbb.bbbb format. A gain of 1.0 is represented by the value of 16.		
R129:2 R0x281	15:0	0x8308	Auto Exposure Day/Night Mode Zones (RW)
	15:10	0x20	Correction Count Correction count that tries to balance the difference between increasing and decreasing exposure steps when a day/ night mode switch is made
	9:5	0x18	Night Mode Auto Exposure Gain Zone Maximum Limit Day mode is determined by whether the value in R0x237[9:5] is different from this value. This field's value is used in the Auto Exposure algorithm.
	4:0	0x8	Day Mode Auto Exposure Gain Zone Maximum Limit This value is determined along with the setting in R0x282[5:0]. Its purpose is annotation, it has no algorithmic purpose within Auto Exposure.
	This register contains the maximum Auto Exposure gain zones for day and night modes. It also contains the correction count register for transitioning between modes.		
R130:2 R0x282	9:0	0x3FC	Auto Exposure Gain Zone 1 Deltas (RW)
	9:5	0x1F	Zone 1 Minimum Delta Signed delta from twice minimum gain (R0x236[7:0]).
	4:0	0x1C	Daylight Mode Maximum Delta Signed delta from maximum gain (R0x236[15:8]).
	These gain entries correspond to minimum and maximum signed deltas from designated base gains for a shutter width of either 1/120 or 1/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed. But since it is assumed that the minimum gain in Zone 1 is exactly minimum gain (R0x236[7:0]) (which makes the delta value zero), the minimum field for this zone is repurposed to hold the delta from maximum gain (R0x236[15:8]) for the last reachable exposure zone of the table (R0x237[9:5]), when that zone is not Zone 24. This helps supports the "Daylight Mode" of auto exposure operation, where it is desired to maintain a frame rate greater than 5 fps, regardless of lighting conditions, by restricting the maximum shutter width.		
R131:2 R0x283	9:0	0x301	Auto Exposure Gain Zone 2 Deltas (RW)
	9:5	0x18	Auto Exposure Gain Zone 2 Maximum Delta Signed delta from twice minimum gain (R0x236[7:0]).
	4:0	0x1	Zone 2 Minimum Delta Signed delta from minimum gain (R0x236[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 2/120 or 2/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R132:2 R0x284	9:0	0xC1	Auto Exposure Gain Zone 3 Deltas (RW)
	9:5	0x6	Zone 3 Maximum Delta Signed delta from minimum gain (R0x236[7:0]).
	4:0	0x1	Zone 3 Minimum Delta Signed delta from minimum gain (R0x236[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 3/120 or 3/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R133:2 R0x285	9:0	0x3A1	Auto Exposure Gain Zone 4 Deltas (RW)
	9:5	0x1D	Zone 4 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1	Zone 4 Minimum Delta Signed delta from Minimum gain threshold (R0x236[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 4/120 or 4/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R134:2 R0x286	9:0	0x3D4	Auto Exposure Gain Zone 5 Deltas (RW)
	9:5	0x1E	Zone 5 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x14	Zone 5 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 5/120 or 5/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R135:2 R0x287	9:0	0x3D7	Auto Exposure Gain Zone 6 Deltas (RW)
	9:5	0x1E	Zone 6 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x17	Zone 6 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 6/120 or 6/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R136:2 R0x288	9:0	0x399	Auto Exposure Gain Zone 7 Deltas (RW)
	9:5	0x1C	Zone 7 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x19	Zone 7 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 7/120 or 7/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R137:2 R0x289	9:0	0x3F8	Auto Exposure Gain Zone 8 Deltas (RW)
	9:5	0x1F	Zone 8 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x18	Zone 8 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 8/120 or 8/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R138:2 R0x28A	9:0	0x1C	Auto Exposure Gain Zone 9 Deltas (RW)
	9:5	0x0	Zone 9 Maximum Delta Zone 9 maximum delta. Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1C	Zone 9 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 9/120 or 9/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R139:2 R0x28B	9:0	0x3BD	Auto Exposure Gain Zone 10 Deltas (RW)
	9:5	0x1D	Zone 10 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1D	Zone 10 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 10/120 or 10/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R140:2 R0x28C	9:0	0x3DB	Auto Exposure Gain Zone 11 Deltas (RW)
	9:5	0x1E	Zone 11 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1B	Zone 11 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 11/120 or 11/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R141:2 R0x28D	9:0	0x3BD	Auto Exposure Gain Zone 12 Deltas (RW)
	9:5	0x1D	Zone 12 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1D	Zone 12 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 12/120 or 12/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R142:2 R0x28E	9:0	0x3FC	Auto Exposure Gain Zone 13 Deltas (RW)
	9:5	0x1F	Zone 13 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1C	Zone 13 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 13/120 or 13/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R143:2 R0x28F	9:0	0x3DE	Auto Exposure Gain Zone 14 Deltas (RW)
	9:5	0x1E	Zone 14 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1E	Zone 14 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 14/120 or 14/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R144:2 R0x290	9:0	0x3DE	Auto Exposure Gain Zone 15 Deltas (RW)
	9:5	0x1E	Zone 15 Maximum Delta Signed delta from gain threshold (R0x238[7:0]).
	4:0	0x1E	Zone 15 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 15/120 or 15/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R145:2 R0x291	9:0	0x3DE	Auto Exposure Gain Zone 16 and 17 Deltas (RW)
	9:5	0x1E	Zone 17 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 17/120 or 17/100 of a second.
	4:0	0x1E	Zone 16 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 16/120 or 16/100 of a second.
	These gain entries correspond to signed deltas from designated base values. Minimum and maximum are identical, therefore deltas for two zones are packed per register.		
R146:2 R0x292	9:0	0x3DE	Auto Exposure Gain Zone 18 and 19 Deltas (RW)
	9:5	0x1E	Zone 19 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 19/120 or 19/100 of a second.
	4:0	0x1E	Zone 18 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 18/120 or 18/100 of a second.
	These gain entries correspond to signed deltas from designated base values. Minimum and maximum are identical; therefore, deltas for two zones are packed per register.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R147:2 R0x293	9:0	0x1F	Auto Exposure Gain Zone 20 and 21 Deltas (RW)
	9:5	0x0	Zone 21 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 21/120 or 21/100 of a second.
	4:0	0x1F	Zone 20 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 20/120 or 20/100 of a second.
	These gain entries correspond to signed deltas from designated base values. Minimum and maximum are identical; therefore, deltas for two zones are packed per register.		
R148:2 R0x294	9:0	0x41	Auto Exposure Gain Zone 22 and 23 Deltas (RW)
	9:5	0x2	Zone 23 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 23/120 or 23/100 of a second.
	4:0	0x1	Zone 22 Delta Signed delta from gain threshold (R0x238[7:0]), for shutter width 22/120 or 22/100 of a second.
	These gain entries correspond to signed deltas from designated base values. Minimum and maximum are identical, therefore deltas for two zones are packed per register.		
R149:2 R0x295	9:0	0x363	Auto Exposure Gain Zone 24 Deltas (RW)
	9:5	0x1B	Zone 24 Maximum Delta Signed delta from maximum gain threshold (R0x236[15:8]).
	4:0	0x3	Zone 24 Minimum Delta Signed delta from gain threshold (R0x238[7:0]).
	These gain entries correspond to minimum and maximum signed deltas from designated base values, for a shutter width of either 24/120 or 24/100 of a second, depending on whether 60Hz or 50Hz power line flicker abatement is assumed.		
R151:2 R0x297	15:0	RO	Luma Saturation Monitor (RO)
	The value of this register is the portion of R0x24C that can be attributed to saturated pixels (those pixels whose luma is equal to or greater than the value in this field.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R154:2 R0x29A	8:0	RO	Dynamic Target Luma Monitor (RO)
	15	RO	Black Alarm If set, indicates that the black alarm has been triggered, which inhibits further decreases in the value of the dynamic target luma.
	14	RO	Dark Limit Set when the scene is too dark for proper exposure.
	13	RO	Bright Limit Set when the scene is too bright for proper exposure.
	12	RO	Auto Exposure Stable Set when Auto Exposure has settled on a proper exposure.
	7:0	RO	Current Target Luma. The current value of the target luma if dynamic target luma is enabled, otherwise the value of the static target luma (R0x22E[7:0]).
	This register reflects the value of the current target luma and the value of the black alarm. The target luma is volatile when the dynamic target luma algorithm is enabled (R0x22F[5] = 1 or R0x29C[5] = 1). Otherwise, it reflects the static value of R0x22E[7:0]. The black alarm is set when Auto Exposure detects an excess of black in the image. An excess is detected when the number of white pixels (controlled by threshold R0x29D[15:8]) plus a fraction of the total number of pixels (controlled by R0x29B[13:8]) is less than the number of black pixels (controlled by threshold R0x29D[7:0]). The black alarm inhibits the dynamic target luma from decreasing beyond its present value.		
R155:2 R0x29B	15:0	0x00D9	Dynamic Target Luma Parameters (RW)
	15:14	0x0	Black Pad This field encodes the portion of total pixels that are added to the count of white pixels in the black alarm heuristic. This sum is then compared against the count of black pixels. If the sum of white count + pad is less than the black count, the black alarm is triggered, and decreases in the dynamic target luma are inhibited. Coding values: 00: 3.0125% of total number of pixels 01: 6.025% of total number of pixels 10: 12.5% of total number of pixels 11: 25% of total number of pixels
	13:8	0x0	Saturated Pixels High Watermark Portion of pixels in saturation that triggers the dynamic target luma algorithm to halt exposure increases. This values compared to the value in the Saturated Pixel Monitor (R0x297[15:8]).
	7:0	0xD9	Reserved.
	This register (along with R0x29D) contains parameters that control the behavior of the Dynamic Target Luma algorithm.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R156:2 R0x29C	15:0	0xD100	Auto Exposure Speed and Sensitivity Control B (RW)
	15	0x1	Auto Exposure Integration Change Decision Delay Delays the next Auto Exposure decision by a frame when the shutter width has changed.
	14	0x1	Auto Exposure Saturated Pixel Adaption Enable Enables Auto Exposure algorithm to boost effort when saturated pixels are present. When a substantial number of saturated pixels are present, the ability to correctly estimate exposures based upon current luminance is reduced.
	13:12	0x1	Auto Exposure Saturated Pixel Adaption Strength Controls how much boost the Auto Exposure algorithm gets when the frame is dominated by saturated pixels. When the saturated pixel measurement indicates that so many pixels are saturated that the target luminance is unreachable through a linear exposure estimate, there is a division by zero condition. This field limits how close to zero the denominator of the Auto Exposure estimate can approach. The value is a power of two, where larger values result in a denominator closer to zero, which in turn results in a larger exposure setting change.
	11	RO	Reserved.
	10	RO	Reserved.
	9	RO	Reserved.
	8:6	0x4	Auto Exposure Adaption Speed Factor of reduction of the difference between current luma and target luma. In one adjustment Auto Exposure advances from current luma to target as follows: 000: 1/4 way going down, 1/8 going up. 001: 1/4 way in both directions. 010: 1/2 way in both directions. 011: 1/2 way going down, 1/4 going up. 100: All the way in both directions (fast adaption). 101: 3/4 way in both directions. 110: 7/8 way in both directions. 111: Reserved.
	5	0x0	Auto Exposure Dynamic Target Enable Dynamic Target Auto Exposure algorithm. If enabled, R0x29C[14] should be set to zero for algorithm stability.
	4:3	0x0	Auto Exposure Decision Frequency Exposure is evaluated every N + 1 frames, where N is given by this field.
	2:0	0x0	Auto Exposure Luma Hysteresis Hysteresis control through time-averaged smoothing of luma data. Luma measurements for Auto Exposure are time-averaged as follows: 000: Auto Exposure luma = current luma. 001: Auto Exposure luma = 1/2 current luma + 1/2 buffered value. 010: Auto Exposure luma = 1/4 current luma + 3/4 buffered value. 011: Auto Exposure luma = 1/8 current luma + 7/8 buffered value. 100: Auto Exposure luma = 1/16 current luma + 15/16 buffered value. 101: Auto Exposure luma = 1/32 current luma + 31/32 buffered value. 110: Auto Exposure luma = 1/64 current luma + 63/64 buffered value. 111: Auto Exposure luma = 1/128 current luma + 127/128 buffered value.
	This register specifies the speed and sensitivity to changes of Auto Exposure in context B. Refer to register R0x22F for the context A version.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R157:2 R0x29D	15:0	0xC50A	Black Alarm Pixel Thresholds (RW)
	15:8	0xC5	Black Alarm White Pixel Threshold Pixel lumas greater than or equal to this value are counted as white pixels. Range is [0–224].
	7:0	0x0A	Black Alarm Black Pixel Threshold Pixel lumas less than or equal to this value are counted as black pixels. Range is [0–224].
	Threshold values for luma that determine whether a pixel is counted as a black or white pixel (or neither) as part of the black alarm heuristic.		
R160:2 R0x2A0	9:0	0xFE	Auto Exposure Maximum Bright Gain Deltas 1 and 2 (RW)
	9:5	0x7	Maximum Gain Delta SW = 2 Maximum gain delta for shutter width equal to 2.
	4:0	0x1E	Maximum Gain Delta SW = 1 Maximum gain delta for shutter width equal to 1.
	Auto Exposure Maximum Bright Gain deltas for shutter widths 1 and 2.		
R161:2 R0x2A1	9:0	0x64	Auto Exposure Maximum Bright Gain Deltas 3 and 4 (RW)
	9:5	0x3	Maximum Gain Delta SW = 4 Maximum gain delta for Shutter width equal to 4.
	4:0	0x4	Maximum Gain Delta SW = 3 Maximum gain delta for shutter width equal to 3.
	Auto Exposure Maximum Bright Gain Deltas for shutter widths 3 and 4.		
R162:2 R0x2A2	9:0	0x42	Auto Exposure Maximum Bright Gain Deltas 5 and 6 (RW)
	9:5	0x2	Maximum Gain Delta SW = 6 Maximum gain delta for shutter width equal to 6.
	4:0	0x2	Maximum Gain Delta SW = 5 Maximum gain delta for shutter width equal to 5.
	Maximum bright gain deltas for shutter width 5 and 6.		
R163:2 R0x2A3	9:0	0x21	Auto Exposure Maximum Bright Gain Deltas 7 and 8 (RW)
	9:5	0x1	Maximum Gain Delta SW = 8 Maximum gain delta for shutter width equal to 8.
	4:0	0x1	Maximum Gain Delta SW = 7 Maximum gain delta for shutter width equal to 7.
	Maximum gain deltas for shutter widths 7 and 8.		
R164:2 R0x2A4	9:0	0x21	Auto Exposure Maximum Bright Gain Deltas 9 and 10 (RW)
	9:5	0x1	Maximum Gain Delta SW = 10 Maximum gain delta for shutter width equal to 10.
	4:0	0x1	Maximum Gain Delta SW = 9 Maximum gain delta for shutter width equal to 9.
	Maximum gain delta for shutter widths equal to 9 and 10.		
R165:2 R0x2A5	5:0	0x0	Auto Exposure Maximum Bright Gain Delta 11 (RW)
	5	0x0	Force Gains Enable Control bit for force gains. If set Auto Exposure uses gains instead of shutter delay when SW < 12, regardless of binning state.
	4:0	0x0	Maximum Gain Delta SW = 11 Maximum gain delta for shutter width equal to 11.
	Auto Exposure Maximum Bright Gain Delta for shutter width 11. Also has the force gains enable bit.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R200:2 R0x2C8	15:0	0x0	Global Context Control (RW)
	15	0x0	Restart sensor on write Controls assertion of sensor restart on update of global context control register. This helps ensure that the very next frame is generated with the new context (a problem with regard to exposure due to the rolling shutter). This bit is automatically cleared once the restart has occurred. 0: Do not restart sensor. 1: Restart sensor.
	14	0x0	Reserved.
	13	0x0	Auto Exposure Speed Context
	12	0x0	Reserved.
	11	0x0	Reserved.
	10	0x0	Resize/Zoom Context Switch resize/zoom contexts: 0: Context A 1: Context B
	9	0x0	OutputFormatCtl2Reg Context Output format control 2 Context. See R0x13A and R0x19B. 0: Context A 1: Context B
	8	0x0	Gamma Table Context R0x153–R0x158 and R0x1DC–R0x1E1. 0: Context A 1: Context B
	7	0x0	Arm Xenon Flash
	6	0x0	Blanking Control This is primarily for use by the internal sequencer when taking automated (for example, flash) snapshots. Setting this bit stops frames from being sent to ensure that the desired frame during a snapshot sequence is the only frame captured by the host. 0: No blanking 1: Blank frames to host
	5	0x0	Reserved.
	4	0x0	Reserved.
	3	0x0	Sensor Read Mode Context (Binning mode, skip mode, power mode (second ADC on/off), see R0x021 and R0x020. 0: Context A 1: Context B

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R200:2 R0x2C8	2	0x0	LED Flash ON 0: Turn off LED Flash 1: Turn on LED Flash
	1	0x0	Vblank Select Vertical blanking context: 0: Context A 1: Context B
	0	0x0	Hblank Select Horizontal blanking context: 0: Context A 1: Context B
	This register defines sensor and colorpipe context for the current frame. Context A is typically used to define preview or viewfinder mode, while context B is typically used for snapshots. The different bits of this register *directly* control their respective functions. If the register is written without synchronization to the frame boundary, this can lead to bad frames. To avoid a bad frame, there are three built-in mechanisms to assist in context-switching: 1. Fully-automatic and single-step programs which are part of the camera-control sequencer. The user runs a built-in program that automates the procedure for switching contexts; see R0x2CC for details. 2. Semi-automatic mode: the user directly controls the contents of this register, but allows built-in mechanism to time the update of this register to avoid a bad frame. This is achieved by writing the value intended for R0x2C8 to R0x2D3 instead. 3. Fully-manual mode: the user can write directly to this register. To avoid a bad frame, the WRITE must be timed to be in vertical blanking and *after* the end-of-frame calculations have completed. See R0x2CA.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R201:2 R0x2C9	7:0	RO	Camera Control Context Status (RO)
	7	RO	Reserved.
	6	RO	Hold AWB Freezes AWB; prevents data collected from the current frame from perturbing the state of color correction.
	5	RO	Hold Auto Exposure Freezes Auto Exposure; prevents data collected from the current frame from perturbing exposure.
	4	RO	Force Xenon Auto Exposure settings Force Auto Exposure Xenon exposure settings. When taking a Xenon snapshot, Auto Exposure cannot actually adapt, but preprogrammed shutter width and gain settings can be used temporarily to control exposure. Refer to R0x2D4.
	3	RO	Auto Exposure Speed Context 0: Use context A version of Auto Exposure Speed and Sensitivity Register (R0x22F) 1: Use context B version of Auto Exposure Speed and Sensitivity Register (R0x29C)
	2:1	RO	Flash Matrix Instructs the AWB unit whether and when to switch from the current color correction settings to the flash settings. 00: No flash matrix. Do not select the flash settings. 01: Conditional loading of flash matrix. Intended primarily for taking LED snapshots, asserting this bit instructs Auto Exposure to use the speed and sensitivity settings in R0x29C. This forces Auto Exposure to aggressively adapt with a goal of settling within three frames. 10: Force flash matrix, that is, unconditional use of the flash matrix. 11: Hold current matrix.
	0	RO	Full frame and Max Line Delay Selector
	This Camera Control Context Status register reflects the operation for the current frame. Typically this register is written to by the Camera Control Sequencer during full-auto or single-step program-advance modes, or reflects indirect writes to R0x2D5, when it takes effect, in either semi-auto or full-manual mode. Refer to R0x2C8 for more details.		
R203:2 R0x2CB	1:0	0x0	Program Advance (RW)
	1	0x0	1: Advance program branch “Advance2.” This field automatically resets to “0” when the advance operation has completed. Writing “1” to this bit is referred to elsewhere as a PA2.
	0	0x0	1: Commence or advance program branch “Advance1.” This field automatically resets to “0” when the advance operation has completed. Writing “1” to this bit is referred to elsewhere as a PA1.
	Writes to this register trigger transitions in the Camera Control function state machine.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R204:2 R0x2CC	5:0	0x0	Program Control (RW)
	5:4	0x0	Program Advance Mode Context Control program execution can be in one of four program advance modes: 00: Full Auto: After PA1 is used to initiate the program, the program automatically advances after each frame, unless a decision state is part of the program, requiring a PA1 or PA2 to continue. 01: Semi-Auto: The user controls the setup for each frame, but the context control updates occur on clean boundaries with respect to frame valid going high or low. 10: Full Manual: The user times context changes, updates are immediate. 11: Single Step: Similar to Full Auto, except that a PA1 is needed to advance the program each frame. In addition, a decision state chooses between PA1 or PA2 to continue.
	3:0	0x0	Program select. 0000: Snapshot: Refer to R0x2CD for parameters. 0001: Snapshot with LED flash: Refer to R0x2CE and R0x2CF for parameters. 0010: Snapshot with Xenon flash: Refer to R0x2D0 and R0x2D4 for parameters. 0011: Video clip: Refer to R0x2D1 for parameters. 0100: Default: Returns to preview settings. Refer to R0x2D2 for parameters. 0101–1111: Reserved.
	This register defines which program is initiated upon writes to "program advance", and defines the current operating mode. Note: The camera resets to, and ends up in, the default mode defined in register R0x2D2 following execution of a program. A program is initiated by writing to "program advance1," R0x2CB[0]. Some programs may require further writes to "program advance1" or “program advance2” (R0x2CB[1]) to advance through certain timing or decision states.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R205:2 R0x2CD	14:0	0x21A0	Snapshot Program Configuration (RW)
	14	0x0	Auto Exposure Speed Context Refer to R0x2C9[3].
	13	0x1	Full Frame and Max Line Delay Selector
	12	0x0	Hold Auto Exposure
	11	0x0	Hold AWB
	10	0x0	Reserved.
	9	0x0	Reserved.
	8	0x1	Resize/ Zoom Context
	7	0x1	OutputFormatCtl2Reg Context
	6	0x0	Gamma Table Context
	5	0x1	Sensor Read Mode Context
	4	0x0	Half-Button State When asserted, snapshot program first transitions to a "half button press" state that is essentially "viewfinder" mode but with Auto Exposure / AWB adaptation turned off.
	3:1	0x0	Number of Frames to Adapt Following optional "half-button press" mode, camera enters "snapshot adapt state." The camera is in full resolution mode with context B resize settings and Auto Exposure / AWB are allowed to adapt. This field defines how many frames to stay in this state. Can be set to 0x0 to bypass state entirely. Frames can be optionally blanked while in this state. Refer to R0x2CD[0]. Following this state, the camera takes a single unblanked snapshot and returns to Default mode / Viewfinder.
	0	0x0	Blank Frames When asserted, frames are blanked during snapshot adapt state; Refer to R0x2CD[3:1].
	This register stores the program configuration for the snapshot without flash. This program cycles through the following states: 0: Preview / Context A initial condition. Trigger a PA1 to advance to state 1 or 2 as a function of R0x2CD[4] 1: Half Button: This state is only entered if R0x2CD[4] is asserted. Refer to detail in R0x2CD[4] description. A PA1 is needed to advance to state 2. 2: Snapshot Adapt: Refer to detail in R0x2CD[3:1]. The sequencer automatically leaves this state after the programmed number of frames and returns to state 0.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R206:2 R0x2CE	15:0	0x1E9B	LED Flash Snapshot Program Configuration (RW)
	15	0x0	Auto Exposure Speed Context (Frame 1) Refer to R0x2C9[3].
	14	0x0	Blank frames during snapshot adaptation. Refer to R0x2C8[6].
	13:12	0x1	Flash Matrix Refer to R0x2C9[2:1] 00: no flash matrix. 01: conditional loading of flash matrix. 10: force flash matrix. 11: hold current matrix.
	11	0x1	Auto Exposure Speed Context (Frame N) Refer to R0x2C9[3].
	10	0x1	Hold Auto Exposure.
	9	0x1	Hold AWB.
	8	0x0	Disable Restart on LED Lag Frame
	7	0x1	Full Frame and Max Line Delay Selector Refer to R0x2C9[0].
	6	0x0	Reserved.
	5	0x0	Reserved.
	4	0x1	Resize/Zoom Context Refer to R0x2C8[10].
	3	0x1	Output Format Control 2 Context Refer to R0x2C8[9].
	2	0x0	Gamma Table Context Refer to R0x2C8[8].
	1	0x1	Sensor Read Mode Context Sensor context. Refer to R0x2C8[0,1,3].
	0	0x1	Lag Frame Controls whether the LED snapshot takes two frames or three frames: 1: Three frames 0: Two frames
	This register holds the parameter configuration for the LED snapshot program. From the current state (for example, context A / preview), a PA1 triggers a fully automated LED flash snapshot. As a function of R0x2CE[0] either two frames (with the second frame being the snapshot) or three frames (with the third frame being the snapshot) are processed before returning to the initial state: 0: Initial state (for example, context A preview). Set R0x2CC = 0x0001 and hit PA1. 1: LED is turned on, R0x2CE[7:1] define the context for this and the subsequent frames. Auto Exposure statistics are collected ready for fast adaptation, and to be input to the decision process of whether to use a flash matrix or not. If R0x2CE[14] = 1 then this frame is blanked. 2: If R0x2CE[0] = 0 then this second frame is the snapshot frame. Exposure settings are applied as a function of R0x2CE[11] and color correction settings are applied as a function of R0x2CE[13:12]. If [R0x2CE[0] = 1 then this is a second frame of adaptation and the frame is conditionally blanked as defined by R0x2CE[14]. 3: If R0x2CE[0] = 1 then this third frame is the snapshot frame. Again, exposure settings are updated and color correction is as defined in R0x2CE[13:12]. 0: Return to the initial state either from state 2 or 3 as a function of R0x2CE[0] The sequencer takes complete control of turning the LED flash on and off. The flash control register (R0x023) should be left at its default value.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R207:2 R0x2CF	15:0	0x4A4A	Auto Exposure/AWB LED Flash Delta Luma Thresholds (RW)
	15:8	0x4A	Luma Threshold to Trigger Shutter Width Zone
	7:0	0x4A	Luma Threshold to Trigger Flash CCM Threshold above which luma must change when LED flash is turned on to trigger a jump to the preset flash CCM; Refer to R0x2C9[2:1] for more information.
	This register holds delta luma threshold values used in the LED snapshot program.		
R208:2 R0x2D0	13:0	0x168D	Xenon Flash Configuration (RW)
	13	0x0	Auto Exposure Speed Context Refer to R0x2C9[3].
	12	0x1	Full Frame and Max Line Delay Selector
	11	0x0	Hold AWB
	10	0x1	Hold Auto Exposure
	9:8	0x2	Flash Matrix 00: no flash matrix. 01: conditional loading of flash matrix. 10: force flash matrix. 11: hold current matrix.
	7	0x1	Force Xenon Auto Exposure Settings
	6	0x0	Extra Frame Needed to compensate if output is double buffered.
	5	0x0	Reserved.
	4	0x0	Reserved.
	3	0x1	Resize/ Zoom Context
	2	0x1	Output Format Control 2
	1	0x0	Gamma Table Context
	0	0x1	Sensor Read Mode Context
	This register stores the parameter configuration for the Xenon snapshot program. This program typically takes a single frame snapshot, firing a Xenon flash between resetting all the sensor rows and reading them out: 0: Initial state. Set R0x2CC = 0x0002 and hit PA1 to advance to state 1. (PA1 is program advance 1.) 1: Switch contexts as defined in R0x2D0[12] and R0x2D0[5:0]. Flash matrix R0x2D0[9:8] is typically set to 0x2 to force the use of the flash color correction matrix and R0x2D0[7] typically is asserted to set up Auto Exposure with the settings defined in R0x2D4. The sensor is then restarted and the Xenon flash armed to fire between the reset and read phases of the rolling shutter. Following the single snapshot frame the sequencer returns to the initial state. Configure the Xenon flash SHUTTER signal duration using R0x023[7:0]. All other bits in R0x023 should be left at their default values.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R209:2 R0x2D1	7:0	0x4D	Video Clip Configuration (RW)
	7	0x0	Auto Exposure Speed Context Refer to R0x2C9[3].
	6	0x1	Full frame and Max Line Delay Selector
	5	0x0	Reserved.
	4	0x0	Reserved.
	3	0x1	Resize/ Zoom Context
	2	0x1	Output Format Control 2 context
	1	0x0	Gamma Table Context
	0	0x1	Sensor Read Mode Context
	Defines the parameter configuration for the video clip program. This simple program allows the user to control the starting and stopping of a video clip through PA1.		
R210:2 R0x2D2	7:0	0x0	Default Program Configuration (RW)
	7	0x0	Auto Exposure Speed Context Refer to R0x2C9[3].
	6	0x0	Full frame and Max Line Delay Selector
	5	0x0	Reserved.
	4	0x0	Reserved.
	3	0x0	Resize/ Zoom Context
	2	0x0	Output Format Control 2 Context
	1	0x0	Gamma Table Context
	0	0x0	Sensor Read Mode Context
	Defines the configuration settings for the preview mode.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R211:2 R0x2D3	15:0	0x0	User Global Context Control (RW)
	15	0x0	Restart Sensor on Write Controls assertion of Sensor Restart on update of Global Context Control Register "1".
	14	0x0	Reserved.
	13	0x0	Auto Exposure Speed Context Refer to R0x2C9[3].
	12	0x0	Reserved.
	11	0x0	Reserved.
	10	0x0	Resize/Zoom Context Switch resize / zoom contexts: 0: Context A. 1: Context B.
	9	0x0	Output Format Control 2 Context 0: OutputFormatCtl2RegA. 1: OutputFormatCtl2RegB.
	8	0x0	Gamma Table Context 0: GammaATable. 1: GammaBTable.
	7	0x0	Arm Xenon Flash
	6	0x0	Blanking Control 0: No blanking. 1: Blank frames to host.
	5	0x0	Reserved.
	4	0x0	Reserved.
	3	0x0	Sensor Read Mode Context Sensor Read Mode context; skip mode, power mode (second ADC on/off). 0: Context A (Read Mode 1 register, R0x021, in sensor selected). 1: Context B (Read Mode 0 register, R0x020, in sensor selected).
	2	0x0	LED Flash ON 0: Turn off LED Flash. 1: Turn on LED Flash.
	1	0x0	Vblank Select Vertical blank context. 0: Context A. 1: Context B.
	0	0x0	Hblank Select Horizontal blank context. 0: Context A. 1: Context B.
	Defines the Sensor and Colorpipe context for the upcoming frame through an indirect update. Updates GCCR (R0x2C8) after Auto Exposure and AWB calculations during vertical blank. Typically this register is written by a driver through the two-wire serial interface while in semi-auto program mode.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R212:2 R0x2D4	14:0	0x209	Xenon Flash Auto Exposure Parameters (RW)
	14:13	0x0	Xenon Flash Snapshot Auto Exposure Saturation Control Auto Exposure Saturation Control for Xenon Flash Snapshot.
	12:5	0x10	Xenon flash Snapshot Auto Exposure Gain Auto Exposure gain setting for Xenon flash snapshots. Recommended range for this virtual gain is 0x10 to 0x80. The virtual gain is translated to sensor analog and IFP digital gains internally.
	4:0	0x9	Xenon Flash Snapshot Auto Exposure Gain Zone Auto Exposure gain zone for Xenon flash snapshot. Typically greater than zone 4 to ensure sufficient time between resetting the sensor rows and reading them out during which the Xenon flash can be fired.
	Defines the Auto Exposure gain, Auto Exposure gain zone index and saturation control gain zone used by the Xenon snapshot program.		
R213:2 R0x2D5	7:0	0x0	Camera Control Context Control (RW)
	7	0x0	Reserved.
	6	0x0	Hold AWB
	5	0x0	Hold Auto Exposure
	4	0x0	Force Xenon Auto Exposure Settings
	3	0x0	Auto Exposure Speed Context Refer to R0x2C9[3].
	2:1	0x0	Flash Matrix 00: no flash matrix. 01: conditional loading of flash matrix. 10: force flash matrix. 11: hold current matrix.
	0	0x0	Full Frame and Max Line Delay Full frame and Max Line Delay selector.
	Defines Camera Control context Status for upcoming frame through an indirect update. Updates CCCR (R0x2C9) at start of vertical blank. Typically written by a driver through the two-wire serial interface while in Semi-Auto or Full Manual program advance modes.		
R214:2 R0x2D6	7:0	0x0	Number of Capture Frame for snapshot (RW)
	Number of Capture Frame for snapshot minus 1.		
R220:2 R0x2DC	15:0	0xFF8	Mg-G Thresholds (RW)
	15:8	0xF	Mg-G Threshold High (signed) Magenta-Green Threshold High (signed).
	7:0	0xF8	Mg-G Threshold Low (signed) Magenta-Green Threshold Low (signed).
	This register contains the limits along the magenta-green axis for the new White Balance chroma test. Values are 8-bit signed numbers in two's complement notation.		
R221:2 R0x2DD	15:0	0x0CE0	B-R Thresholds (RW) (Blue-Red)
	15:8	0x0C	B-R Threshold High (signed)
	7:0	0xE0	B-R Threshold Low (signed)
	This register contains the limits along the blue-red axis for the new White Balance chroma test. Values are 8-bit signed numbers in two's complement notation.		

Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R222:2 R0x2DE	0:0	0x1	New Chroma Test Enable (RW)
	Enables the new chroma test, which compares the chromas of each pixel against a rectangle aligned to the Magenta-Green and Blue-Red axes in U-V space.		
R239:2 R0x2EF	5:0	0x8	AWB Advanced Control 2 (RW)
	5:3	0x1	White Balance Block Size Threshold 000: AWB Always enabled. 001: AWB is disabled if block size is below 8x8. 010: AWB is disabled if block size is below 16x16. 011: AWB is disabled if block size is below 32x32. 100: AWB is disabled if block size is below 64x64. 101-111: Reserved. Auto White Balance is disabled below specified block size. Refer to R0x22D for more details.
	2:0	0x0	Gain Adjustment Smoothing for Flash Specify maximum gain change per adjustment when using flash: 000: current gain = new gain. 001: current gain = 1/2 new gain + 1/2 old gain. 010: current gain = 1/4 new gain + 3/4 old gain. 011: current gain = 1/8 new gain + 7/8 old gain. 100: current gain = 1/16 new gain + 15/16 old gain. 101: current gain = 1/32 new gain + 31/32 old gain. 110: current gain = 1/64 new gain + 63/64 old gain. 111: current gain = 1/128 new gain + 127/128 old gain.
	This register stores additional controls for the AWB algorithm.		
R240:2 R0x2F0	2:0	0x0	Page Map (RW)
	2:0	0x0	Page Address: 000: Sensor address page. 001: Colorpipe Address page. 010: Camera control address page. 011–111: Reserved.
	This register specifies the memory address page for the two-wire interface protocol.		
R241:2 R0x2F1	15:0	0x0	Byte Wise Address (RW)
	Use this register to perform reads and writes to the sensor in two 8-bit serial transmissions instead of one 16-bit.		
R242:2 R0x2F2	15:0	0x0	AWB Digital Gain Offsets (RW)
	15:8	0x0	Red Gain Offset Red digital gain offset.
	7:0	0x0	Blue Gain Offset Blue digital gain offset.
	This register stores the red and blue digital gain offsets used when auto white balance is enabled (R0x206[1] = 1). These 8-bit offsets are represented in b.bbbbbbb fixed point.		
R245:2 R0x2F5	7:0	0x40	Manual White Balance Matrix Position (RW)
	This register stores the matrix position to use for manual White Balance. The position is a 7-bit number represented in 0.bbbbbbb fixed point. Positions range from 0/128 for red-rich illumination to 127/128 for blue-rich illumination.		
R246:2 R0x2F6	7:0	0x7F	Flash White Balance Matrix Position (RW)
	This register stores the matrix position to use for White Balance with flash. The position is a 7-bit number represented in 0.bbbbbbb fixed point. Positions range from 0/128 for red-rich illumination to 127/128 for blue-rich illumination.		

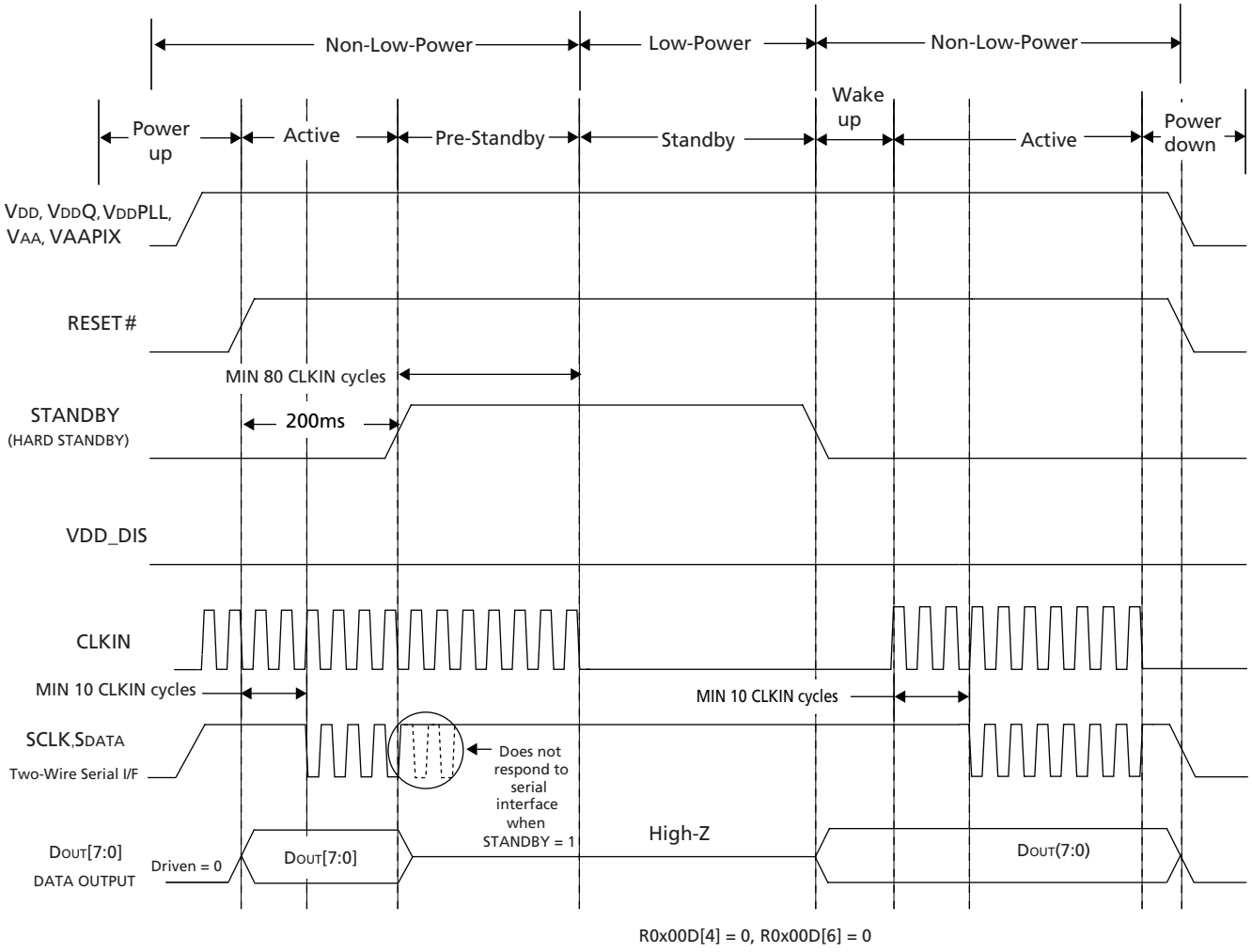
Table 17: Page 2: Camera Control Register Descriptions (continued)
Data format: RO = Read Only; RW = Read/Write (R/W); Hex = Hexadecimal; – = Reserved; X = Indeterminate

Reg # Decimal Hex	Bits	Default	Description
R255:2 R0x2FF	15:0	0xA880	White Balance Flash Gains (RW)
	15:8	0xA8	Red Flash Gain Starting red digital gain for flash.
	7:0	0x80	Blue Flash Gain Starting blue digital gain for flash.
	This register stores the red and blue digital gains that serve as the starting gains when the flash matrix is in use. The 8-bit values represent the gains in b.bbbbbbb fixed point. Values range from 0/128 to 255/128.		

Reset, Clocks, and Low Power Modes

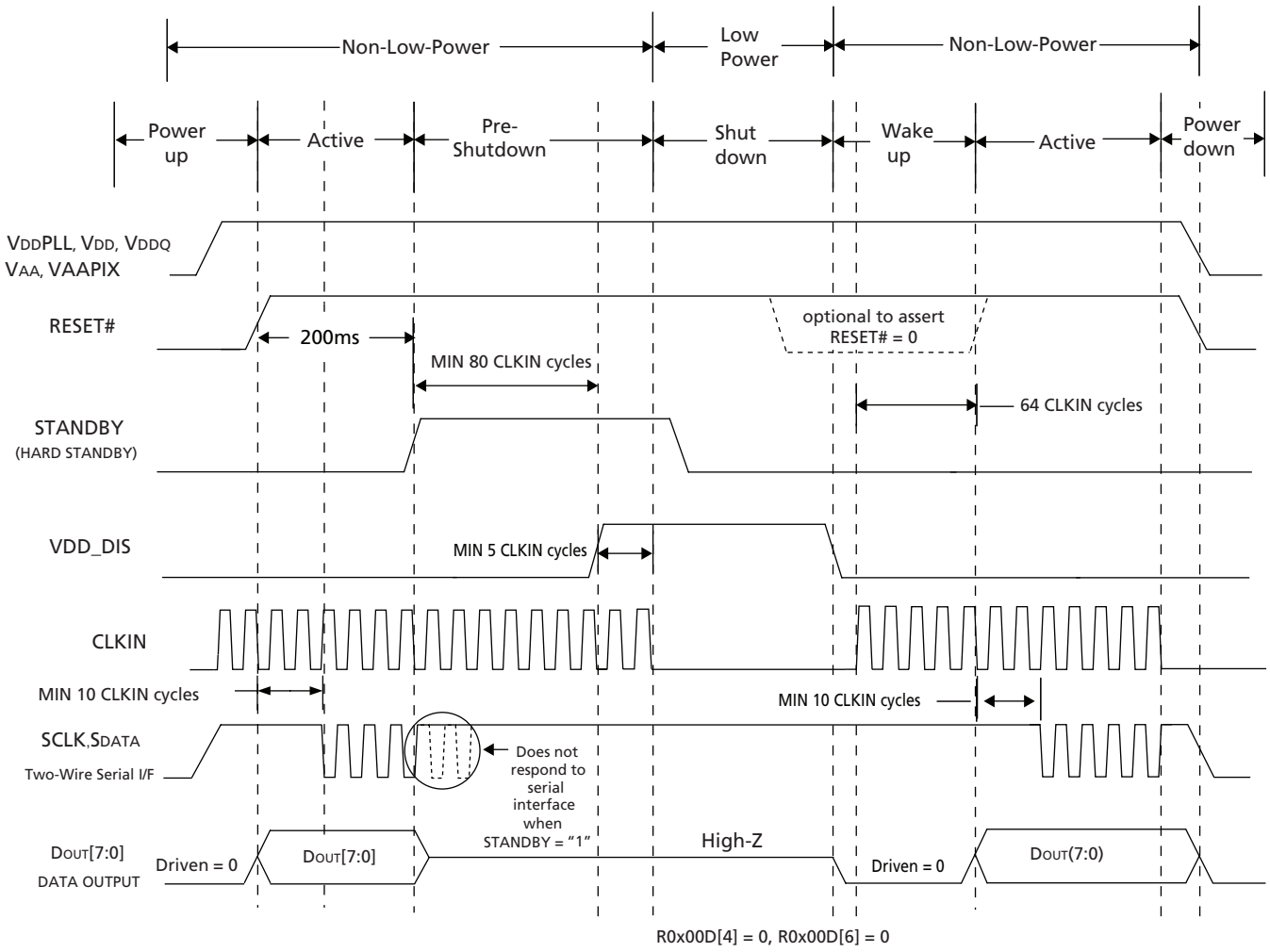
There are no constraints concerning the order in which the various power supplies are applied; however, the MT9M112 requires reset in order to operate properly at power-up. Refer to the Figure 6 for the power-up, reset, and standby sequences.

Figure 6: Power-Up, Reset, Clock, and Standby Sequence



Notes:
1. All output signals are defined during initial power-up with RESET# = 0 without CLKIN being active. For a proper reset sequence for the rest of the sensor, during initial powerup, assert RESET# = 0 for at least 1µS after all power supplies have stabilized and CLKIN is active (being clocked). Driving RESET# = 0 does not put the part in a low power state.
2. In Hard standby the output signals are high impedance by default. The output state is controlled by register R0x00D settings.
3. Soft standby is asserted or deasserted by a two-wire serial interface to R0x00D[2]. In this mode, the analog clock and the internal clocks are shut off. The output signals are not high impedance by default. The total leakage currents can be lowered if the two-wire serial interface and the CLKIN are turned OFF after 80 CLKIN cycles after issuing soft standby.
4. Wait for 10 CLKIN rising edges after RESET# is deasserted before using two-wire serial interface.
5. Illustration not drawn to scale (do not count number of clock pulses).

Figure 7: VDD_DIS Shutdown Sequence



Note: Illustration not drawn to scale (do not count number of clock pulses).

VDD Disable Feature

The VDD_DIS signal is used to shut down digital core VDD reducing the power consumption significantly during standby. All register settings are lost. However, the output signal states are maintained as long as VDDQ is maintained. Output signals must be configured appropriately during the standby sequence. Input signal transitions (including RESET#) during VDD_DIS = 1 are ignored.

Proper shutdown and recovery sequences must be followed for minimum power consumption.

Disable and enable the core VDD using the VDD_DIS signal with the following sequences.

To Enter Low Power State

1. PLL bypass R0x065[15] = 1
2. PLL into standby/power down
3. Enter standby mode (hardware or software)
4. Assert VDD_DIS
5. Stop CLKIN
6. Deassert STANDBY if asserted
7. The part is now in a core VDD shutdown low power state

To Exit Low Power State

1. Assert RESET# (optional)
2. Assert STANDBY if the output must be high impedance during start-up
3. Deassert VDD_DIS
4. Start CLKIN
5. Deassert RESET# (if asserted in step 1 above) and start up the sensor

PLL Operation

The sequence to turn on PLL is:

1. After the chip power on reset, PLL is in bypass mode by default.
2. Program PLL parameters M, N, and P in R0x066 and R0x067 depending on the external clock frequency and target clock frequency. PLL output clock frequency (^{f}OUT) is calculated with the following equation:

$$f_{OUT} = f_{CLKIN} \times M \times \left(\frac{1}{2 \times (N+1) \times (P+1)} \right) \quad \text{(EQ 1)}$$

   Where ^{f}CLKIN is external clock frequency, N is pre-divider and P is post-divider. Both registers have a default value of "1."
3. Wake up PLL by programming R0x065[14] = 0.
4. Wait at least 1ms for PLL to stabilize.
5. Program R0x065[15] = 0 to enable PLL output to clock core and release PLL bypass.

Electrical Specifications

DC Electrical Specification

Table 18 defines the main power supply voltages and operating conditions of the MT9M112.

Table 18: DC Electrical Characteristics and Operating Conditions
Setup conditions: T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
VDD	Core digital voltage		1.7	1.8	1.9	V
VDDQ	I/O digital voltage		1.7	1.8V or 2.8V	3.1	V
VAA	Analog voltage		2.5	2.8	3.1	V
VAAPIX	Pixel supply voltage		2.5	2.8	3.1	V
VDDPLL	PLL analog voltage		2.5	2.8	3.1	V
	Leakage current	STANDBY = VDDQ (asserted) VDD_DIS = VDDQ (asserted) CLKIN = 0V (no clocks running)	–	–	10	µA
		STANDBY = VDDQ (asserted) VDD_DIS = 0V (deasserted) CLKIN = 0V (no clocks running)	–	–	300	µA
	Operating power consumption[1]	SXGA @ 15 fps	–	–	170	mW
		VGA @ 30 fps, binning enabled	–	–	100	
T_J	Operating junction temperature		-30	–	+70	°C

Note: 1. Power consumption numbers do not include power from VDDQ.

I/O Parameters

Table 19 and Table 20 define threshold parameters for voltage and current on input and output signals.

Table 19: I/O Min/Max Parameters (V_{DDQ} = 1.8V)

Setup conditions: V_{DD} = 1.8V, V_{DDQ} = 1.8V, V_{AA} = 2.8V, VAAPIX = 2.8V, V_{DDPLL} = 2.8V, T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	MIIN	MAX	Unit
V_{IH}	Input high voltage	I_{IH} = -10 µA	1.7	–	V
V_{IL}	Input low voltage	I_{IL} = 10 µA	–	0.3	V
V_{OH}	Output high voltage	I_{OH} = -9mA	V_{DDQ} - 0.4	–	
V_{OL}	Output low voltage	I_{OL} = 9mA	–	0.4	
I_{OH}	Output high current	V_{OH} = 1.5V	–	-6	mA
I_{OL}	Output low current	V_{OL} = 0.3V	–	6	mA
I_L	Input leakage current	V_{IN} = 0V or V_{DDQ} all signals including output pins in high impedance state	–	±5	µA
		V_{IN} = 3.1V; V_{DD} = 0V, V_{DDQ} = 0V, V_{AA} = 0V, VAAPIX = 0V, V_{DDPLL} = 0V SDATA and SCLK signals only	–	±5	µA

Table 20: I/O Min/Max Parameters (V_{DDQ} = 2.8V)

Setup conditions: V_{DD} = 2.8V, V_{DDQ} = 2.8V, V_{AA} = 2.8V, VAAPIX = 2.8V, V_{DDPLL} = 2.8V, T_J = -30°C to +70°C, unless specified otherwise

Symbol	Definition	Condition	MIIN	MAX	Unit
V_{IH}	Input high voltage	I_{IH} = -10 µA	2.5	–	V
V_{IL}	Input low voltage	I_{IL} = 10 µA	–	0.3	V
V_{OH}	Output high voltage	I_{OH} = -15mA	V_{DDQ} - 0.4	–	V
V_{OL}	Output low voltage	I_{OL} = 15mA	–	0.4	V
I_{OH}	Output high current	V_{OH} = 2.5V	–	-11	mA
I_{OL}	Output low current	V_{OL} = 0.3V	–	11	mA
I_L	Input leakage current	V_{IN} = 0V or V_{DDQ} all signals including output pins in high impedance state	–	±5	µA
		V_{IN} = 3.1V; V_{DD} = 0V, V_{DDQ} = 0V, V_{AA} = 0V, VAAPIX = 0V, V_{DDPLL} = 0V SDATA and SCLK signals only	–	±5	µA

AC Electrical Specification

Figure 8 and Figure 9 illustrate clock and I/O timing and show the timing relationships that are defined in Table 21 on page 106.

Figure 8: Clock Rise and Fall Timing

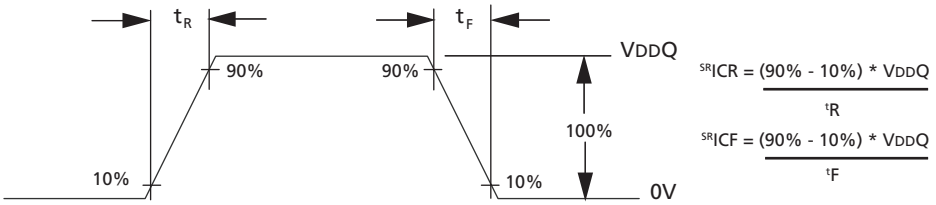
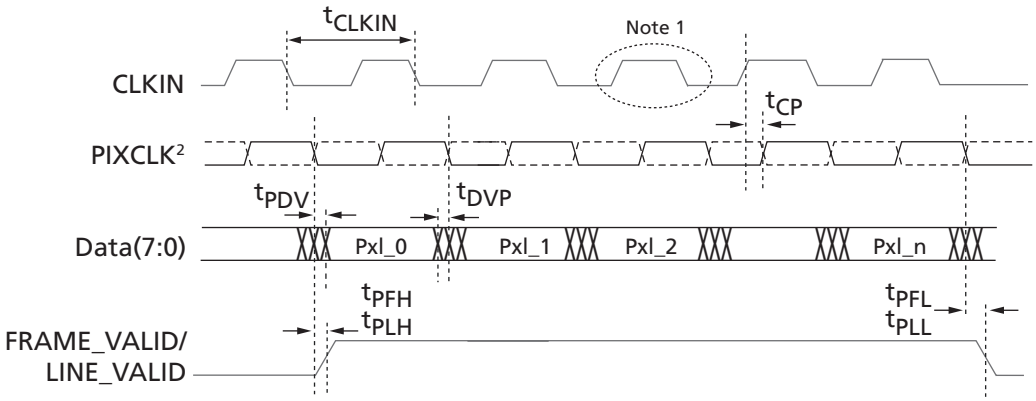


Figure 9: I/O Timing Diagram



Notes: 1. See Figure 8 for Rise and Fall Timing details.
2. PLL disabled for tCP. PIXCLK is in phase with CLKIN with propagation delay of tCP by default (solid line) and could be inverted (dashed line).

Timing Parameters (1.8V)

Table 21 defines timing parameters for the main clocks and the timing relationship between clocks and valid data.

Table 21: I/O Timing Parameters (V_{DDQ} = 1.8V)[1]

AC Setup Conditions: ^{f}CLKIN = 48 MHz, V_{DD} = 1.8V, V_{DDQ} = 1.8V, V_{AA} = 2.8V, VAAPIX = 2.8V, V_{DD}PLL = 2.8V, Output Load = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
^{f}CLKIN1	Input clock frequency	PLL enabled	6	48	54	MHz
^{t}CLKIN1	Input clock period	PLL enabled	18.5	20.8	166.6	ns
^{f}CLKIN2	Input clock frequency	PLL disabled	6	48	54	MHz
^{t}CLKIN2	Input clock period	PLL disabled	18.5	20.8	166.6	ns
^{SR}ICR[3]	Input clock rising edge slew rate	CLKIN = 54 MHz	0.70	–	–	V/ns
		CLKIN = 27 MHz	0.40	–	–	V/ns
		CLKIN = 13.5 MHz	0.23	–	–	V/ns
^{SR}ICF[3]	Input clock falling edge slew rate	CLKIN = 54 MHz	0.70	–	–	V/ns
		CLKIN = 27MHz	0.40	–	–	V/ns
		CLKIN = 13.5MHz	0.23	–	–	V/ns
^{D}CLKIN	Input clock duty cycle	CLKIN = 54 MHz	45	50	55	%
^{t}JITTER	Input clock jitter	CLKIN = 54 MHz	–	–	0.15	ns
^{t}CP	CLKIN to PIXCLK propagation delay	PLL disabled	–	12	–	ns
^{f}PIXCLK	PIXCLK frequency	PLL enabled or disabled	6	48	54	MHz
^{D}PIXCLK	PIXCLK output duty cycle	PLL enabled or disabled	40	50	60	%
^{t}PDV	PIXCLK to data valid		-2	–	2	ns
^{t}DVP	Data valid to PIXCLK		-2	–	2	ns
^{t}PFH	PIXCLK to FV HIGH		-2	–	2	ns
^{t}PLH	PIXCLK to LV HIGH		-2	–	2	ns
^{t}PFL	PIXCLK to FV LOW		-2	–	2	ns
^{t}PLL[2]	PIXCLK falling edge to LV falling edge		39.7	–	43.7	ns
C_{IN}	Input signal capacitance		–	3.5	–	pF
C_{LOAD}	Load capacitance		–	–	30	pF

Notes:
1. Output signals D_{OUT}(7:0), LINE_VALID (LV), and FRAME_VALID (FV) are not synchronized with PIXCLK and thus may lag or lead PIXCLK. Therefore, ^{t}PDV, ^{t}DVP, ^{t}PFH, ^{t}PLH, and ^{t}PFL may be positive or negative.
2. Two PIXCLK cycles are missing prior to falling edge of LV. ^{t}PLL for PIXCLK = 48 MHz.
3. Slew rates for input clock rising edge (^{SR}ICR) and falling edge (^{SR}ICF) should not differ by more than 10%.

Timing Parameters (2.8V)

Table 22: I/O Timing Parameters (V_{DDQ} = 2.8V)[1]

AC Setup Conditions: ^{f}CLKIN = 48 MHz, V_{DD} = 1.8V, V_{DDQ} = 2.8V, V_{AA} = 2.8V, VAAPIX = 2.8V, V_{DD}PLL = 2.8V, Output Load = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Symbol	Definition	Condition	MIN	TYP	MAX	Unit
^{f}CLKIN1	Input clock frequency	PLL enabled	6	48	54	MHz
^{t}CLKIN1	Input clock period	PLL enabled	18.5	20.8	166.6	ns
^{f}CLKIN2	Input clock frequency	PLL disabled	6	48	54	MHz
^{t}CLKIN2	Input clock period	PLL disabled	18.5	20.8	166.6	ns
^{SR}ICR[3]	Input clock rising edge slew rate	CLKIN = 54 MHz	1.10	–	–	V/ns
		CLKIN = 27 MHz	0.62	–	–	V/ns
		CLKIN = 13.5 MHz	0.36	–	–	V/ns
^{SR}ICF[3]	Input clock falling edge slew rate	CLKIN = 54 MHz	1.10	–	–	V/ns
		CLKIN = 27MHz	0.62	–	–	V/ns
		CLKIN = 13.5MHz	0.36	–	–	V/ns
^{D}CLKIN	Input clock duty cycle	CLKIN = 54 MHz	45	50	55	%
^{t}JITTER	Input clock jitter	CLKIN = 54 MHz	–	–	0.15	ns
^{t}CP	CLKIN to PIXCLK propagation delay	PLL disabled	–	12	–	ns
^{f}PIXCLK	PIXCLK frequency	PLL enabled or disabled	6	48	54	MHz
^{D}PIXCLK	PIXCLK output duty cycle	PLL enabled or disabled	40	50	60	%
^{t}PDV	PIXCLK to data valid		-2	–	2	ns
^{t}DVP	Data valid to PIXCLK		-2	–	2	ns
^{t}PFH	PIXCLK to FV HIGH		-2	–	2	ns
^{t}PLH	PIXCLK to LV HIGH		-2	–	2	ns
^{t}PFL	PIXCLK to FV LOW		-2	–	2	ns
^{t}PLL[2]	PIXCLK falling edge to LV falling edge		39.7	–	43.7	ns
C_{IN}	Input signal capacitance		–	3.5	–	pF
C_{LOAD}	Load capacitance		–	–	30	pF

Notes:
1. Output signals D_{OUT}(7:0), LINE_VALID (LV), and FRAME_VALID (FV) are not synchronized with PIXCLK and thus may lag or lead PIXCLK. Therefore, ^{t}PDV, ^{t}DVP, ^{t}PFH, ^{t}PLH, and ^{t}PFL may be positive or negative.
2. Two PIXCLK cycles are missing prior to falling edge of LV. ^{t}PLL for PIXCLK = 48 MHz.
3. Slew rates for input clock rising edge (^{SR}ICR) and falling edge (^{SR}ICF) should not differ by more than 10%.

Output Signal Slew Rate Control (1.8V)

Table 23 and Table 24 show the codes for adjusting the slew rate of output signals.

Table 23: Output Signal Slew Rate (1.8V)

Setup conditions: V_{DDQ} = 1.8V, Output Load C_{LOAD} = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Signals	Parameter	Definition	MIN	TYP	MAX	Unit
DOUT[7:0], FV, LV, FLASH, SHUTTER, PIXCLK, SDATA	SRHL, SRLH	Output slew rate, code 0, Slowest	0.12	–	0.14	V/ns
		Code 1	0.13	–	0.16	
		Code 2	0.14	–	0.17	
		Code 3	0.16	–	0.19	
		Code 4	0.18	–	0.22	
		Code 5	0.20	–	0.25	
		Code 6	0.24	–	0.29	
		Code 7, Fastest	0.30	–	0.35	

Output Signal Slew Rate Control (2.8V)

Table 24: Output Signal Slew Rate (2.8V)

Setup conditions: V_{DDQ} = 2.8V, Output Load C_{LOAD} = 15pF, T_J = -30°C to +70°C, unless otherwise specified.

Signals	Parameter	Definition	MIN	TYP	MAX	Unit
DOUT[7:0], FV, LV, FLASH, SHUTTER, PIXCLK, SDATA	SRHL, SRLH	Output slew rate, code 0, Slowest	0.32	–	0.35	V/ns
		Code 1	0.37	–	0.41	
		Code 2	0.42	–	0.46	
		Code 3	0.48	–	0.52	
		Code 4	0.58	–	0.63	
		Code 5	0.73	–	0.78	
		Code 6	0.97	–	1.05	
		Code 7, Fastest	1.65	–	1.73	

Two-Wire Serial Interface Specification

The following diagrams illustrates the Two-Wire Serial Interface bus timing.

Figure 10: Two-Wire Serial Interface Timing Diagram

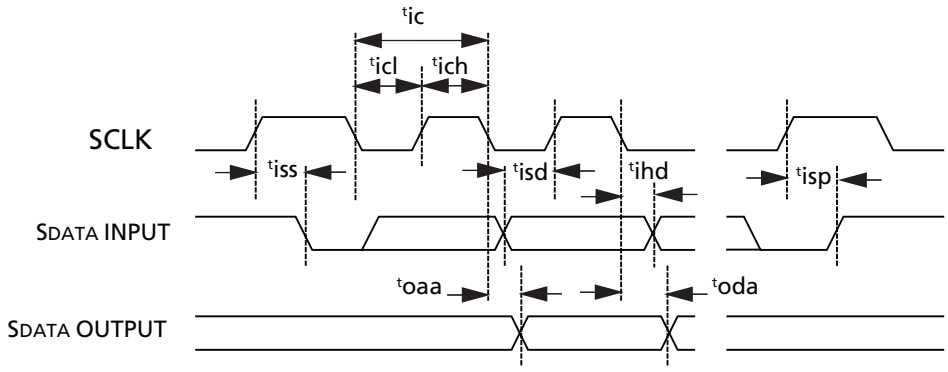


Figure 11: Two-Wire Serial Interface Start and Stop Condition Timing

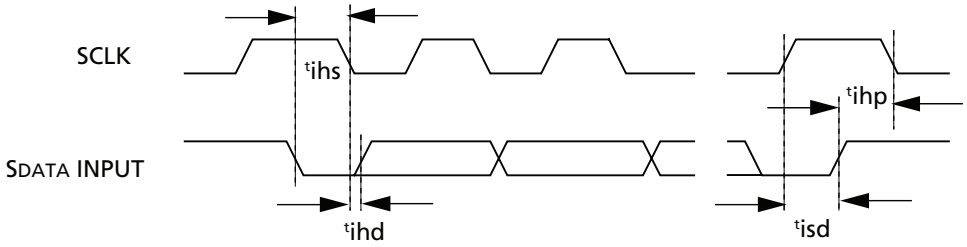


Table 25: Two-Wire Serial Interface Timing

^{f}SCLK = 400KHz, V_{DD} = 1.8V, V_{AA} = 2.8V, VAAPIX = 2.8V, $V_{DD}Q$ = 2.8V, T_J = -30°C to +70°C, unless otherwise specified.

SYMBOL	DEFINITION	MIN	TYPICAL	MAX	UNITS
^{f}SCLK	Two-Wire Serial Interface Input clock frequency			400	KHz
^{t}ic	Two-Wire Serial Interface Clock period	2500			ns
^{t}ich	Two-Wire Serial Interface Clock period High		1250		ns
^{t}icl	Two-Wire Serial Interface Clock period Low		1250		ns
^{t}iss	Setup time for start condition	625			ns
^{t}ihs	Hold time for start condition	416.7			ns
^{t}isd	Setup time for input data	625			ns
^{t}ihd	Hold time for input data	625			ns
^{t}oaa	Output data acknowledge time	1250			ns
^{t}oda	Output data delay time	1250			ns
^{t}isp	Setup time for stop condition	625			ns
^{t}ihp	Hold time for stop condition	625			ns
^{C}INSI	Serial interface input pin capacitance		3.5		pF
^{C}LOADSD	SDATA max load capacitance			30	pF
^{R}SD	SDATA pull-up resistor		1.5		KΩ

Absolute Maximum Ratings

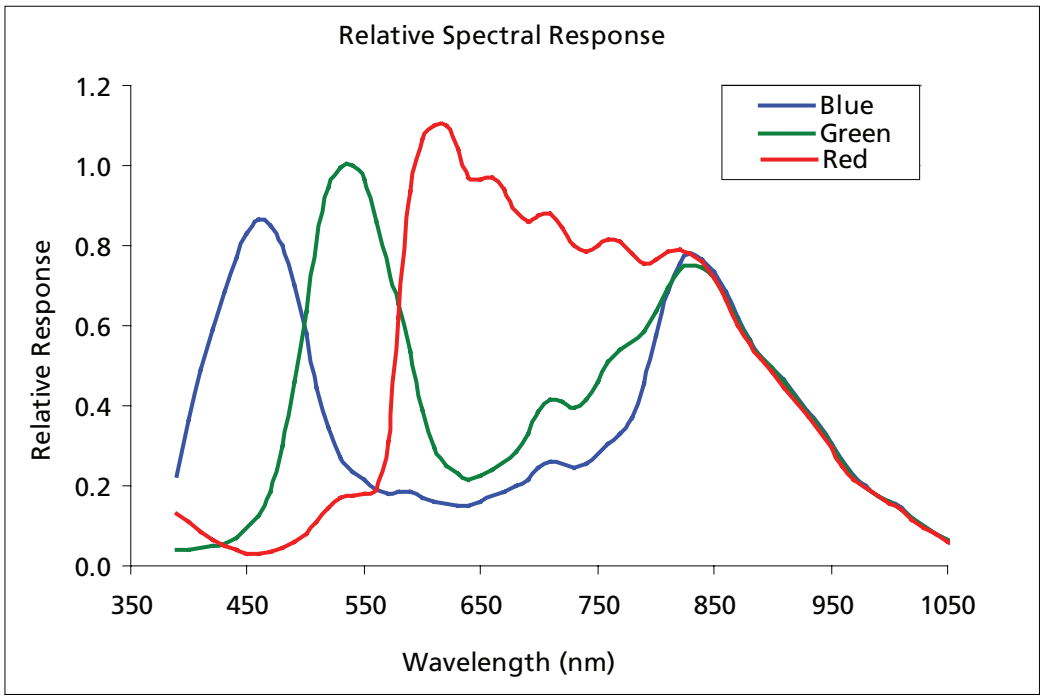
Table 26: Absolute Maximum Ratings

Symbol	Definition	Condition	MIN	MAX	Unit
VSUPPLY	Power supply voltage (all supplies)	DGND=0V, AGND=0V	-0.3	4.0	V
ISUPPLY	Total power supply current		–	150	mA
IGND	Total GND current		–	150	mA
VIN	DC Input voltage	All signals except SDATA and SCLK	-0.3	VDDQ + 0.3	V
		SDATA and SCLK signals, VDDQ = 0V	-0.3	3.6	V
VOUT	DC output voltage		-0.3	VDDQ + 0.3	V
TSTG	Storage temperature		-40	+85	°C

Note: Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Spectral Characteristics

Figure 12: Typical Spectral Characteristics



Revision History

Rev. B, Preliminary 12/05

- Updated register summary, see "Sensor Core Registers – Summary" on page 22
- Updated detailed register tables, see "Page 0: Sensor Core Register Descriptions" on page 33, "Page 1: Image Processing Register Descriptions" on page 48 and "Page 2: Camera Control Register Descriptions" on page 64
- Updated electrical specifications, see "Electrical Specifications" on page 103

Rev. A, Advance 4/05

- Initial release